

# LOW-DISTORTION 1.6 TO 30 MHz SSB DRIVER DESIGNS

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## GENERAL CONSIDERATION

Two of the most important factors to be considered in broadband linear amplifier design are the distortion and the output harmonic rejection.

The major cause for intermodulation distortion is amplitude nonlinearity in the active element. The nonlinearity generates harmonics, and the fundamental odd-order products are defined as  $2f_1 - f_2$ ,  $2f_2 - f_1$ ,  $3f_2 - 2f_1$ , etc., when a two-tone test signal is used. These harmonics may not always appear in the amplifier output due to filtering and cancellation effects, but are generated within the active device. The amplitude and harmonic distortion cannot really be distinguished, except in a case of a cascaded system, where even-order products in each stage can produce odd-order products through mixing processes that fall in the fundamental region.<sup>2</sup> This, combined with phase distortion — which in practical circuits is more apparent at higher frequencies — can make the distortion analysis extremely difficult;<sup>5,2</sup> whereas, if only amplitude distortion was present, the effect of IMD in each stage could easily be calculated.

In order to expect a low harmonic output of the power amplifier, it is also important for the driving source to be harmonic-free. This is difficult in a four-octave bandwidth system, even at 10 – 20 watt power levels. Class A biasing helps the situation, and Class A push-pull yields even better results due to the automatic rejection of even harmonics.

Depending on the application, a full Class A system is not always feasible because of its low efficiency. The theoretical maximum is 50%, but practical figures are not higher than 25% to 35%. It is sometimes advantageous to select a bias point somewhere between Class AB and A which would give sufficiently good results, since filtering is required in the power amplifier output in most instances anyway.

In order to withstand the high level of steady dc bias current, Class A requires a much larger transistor die than Class B or AB for a specific power output. There are sophisticated methods such as generating the bias voltage from rectified RF input power, making the dc bias proportional to the drive level.<sup>1</sup> This also yields to a better efficiency.

## 20 W, 25 dB AMPLIFIER WITH LOW-COST PLASTIC DEVICES

The amplifier described here provides a total power gain of about 25 dB, and the construction technique allows the use of inexpensive components throughout. The plastic RF power transistors, MRF475 and MRF476, featured in this amplifier, were initially developed for the CB market. The high manufacturing volume of these TO-220 packaged parts

makes them ideal for applications up to 50 MHz, where low cost is an important factor.

The MRF476 is specified as a 3-watt device and the MRF475 has an output power of 12 watts. Both are extremely tolerant to overdrive and load mismatches, even under CW conditions. Typical IMD numbers are better than -35 dB, and power gains are 18 dB and 12 dB, respectively, at 30 MHz.

The collectors of the transistors are electrically connected to the TO-220 package mounting tab which must be isolated from the ground with proper mounting hardware (TO-220 AB) or by floating heat dissipators. The latter method, employing Thermalloy 6107 and 6106 heat dissipators, was adapted for this design. Without an airflow, the 6106 and 6107 provide sufficient heat sinking for about 30% duty cycle in the CW mode. Collector idle currents of 20 mA are recommended for both devices, but they were increased to 100 mA for the MRF475 and to 40 mA for the MRF476 to reduce the higher order IMD products and to achieve better harmonic suppression.

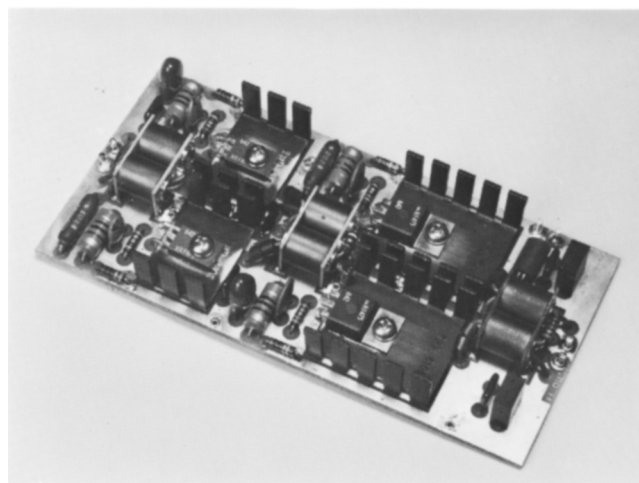
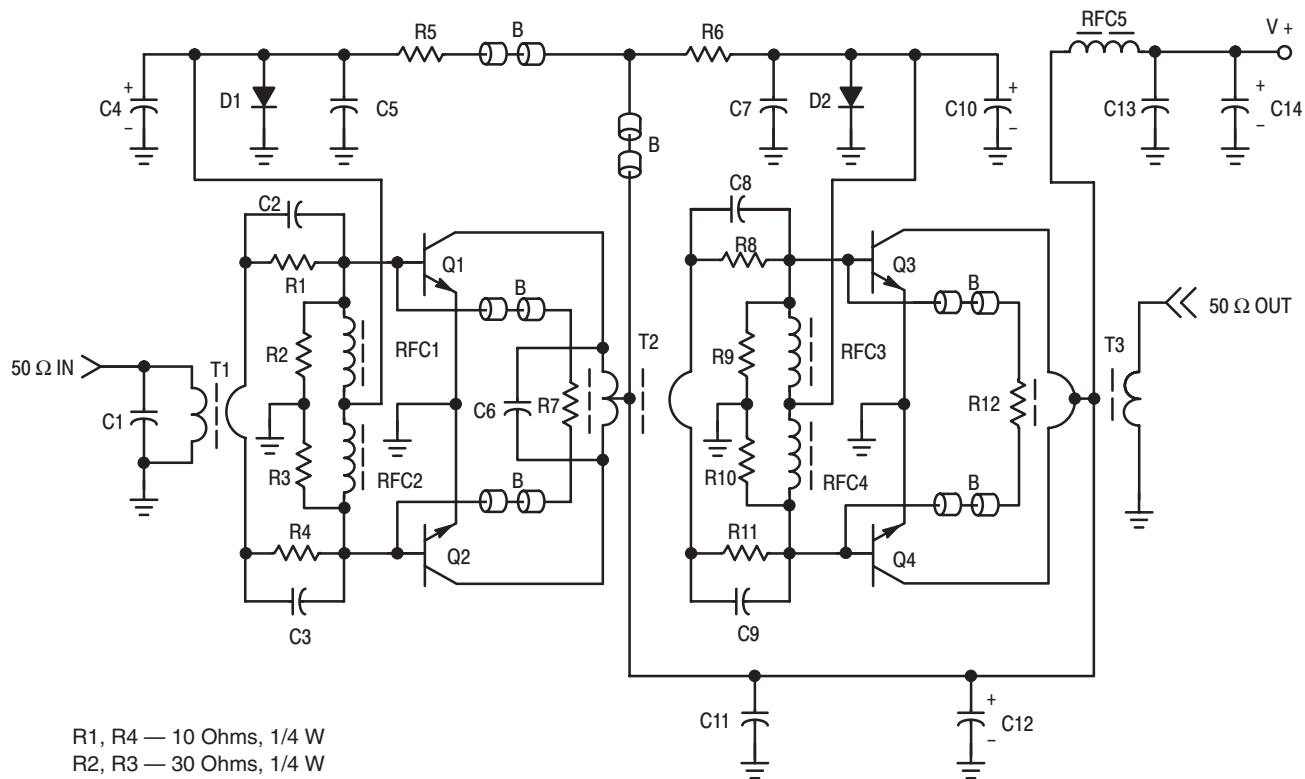


Figure 1.

## Biasing and Feedback

The biasing is achieved with the well-known clamping diode arrangement (Figure 2). Each stage has its own diode, resistor, and bypass network, and the diodes are mounted between the heat dissipators, being in physical contact with them for temperature-tracking purposes. A better thermal contact is achieved through the use of silicone grease in these junctions.

The bias currents of each stage are individually adjustable with R5 and R6. Capacitors C4 and C10 function as audio-frequency bypasses to further reduce the source impedance at the frequencies of modulation.



R1, R4 — 10 Ohms, 1/4 W  
 R2, R3 — 30 Ohms, 1/4 W  
 R5, R6 — 82 Ohms, 3 W (Nom.)  
 R7 — 47 Ohms, 1/4 W  
 R8, R11 — 6.8 Ohms, 1/4 W  
 R9, R10 — 15 Ohms, 1/4 W  
 R12 — 130 Ohms, 1/4 W  
 C1 — 39 pF Dipped Mica  
 C2, C3 — 680 pF Ceramic Disc  
 C4, C10 — 220  $\mu$ F, 4 V, Tantalum  
 C5, C7, C11, C13 — 0.1  $\mu$ F Ceramic Disc  
 C6 — 56 pF Dipped Mica  
 C8, C9 — 1200 pF Ceramic Disc  
 C12, C14 — 10  $\mu$ F, 25 V Tantalum

RFC5 — Ferroxcube V K200 19/4B  
 RFC1, 2, 3, 4 — 10  $\mu$ H Molded Choke  
 B — Ferrite Beads (Fair-Rite Prod. Corp. #2643000101 or Ferroxcube #56 590 65/3B)  
 D1, D2 — 1N4001  
 Q1, Q2 — MRF476  
 Q3, Q4 — MRF475  
 T1, T2 — 4:1 Impedance Transformer  
 T3 — 1:4 Impedance Transformer

**Figure 2. Schematic and Components Parts List**

\* NOTE: Parts and kits are available from Communication Concepts Inc., 508 Millstone Drive, Beavercreek, Ohio 45434-5840 (513) 426-8600

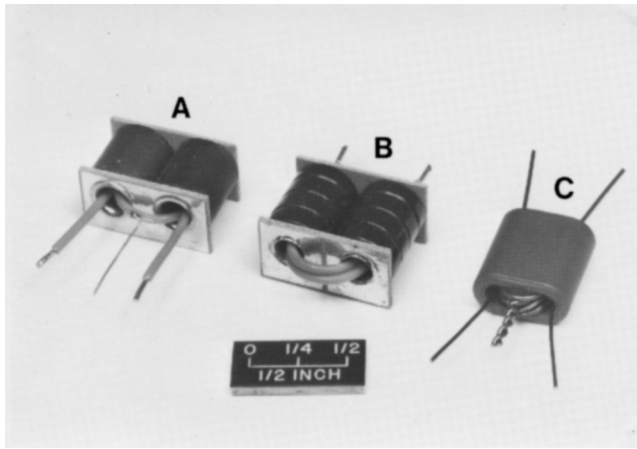
This biasing arrangement is only practical in low and medium power amplifiers, since the minimum current required through the diode must exceed  $I_C/h_{fe}$ .

Gain leveling across the band is achieved with simple RC networks in series with the bases, in conjunction with negative feedback. The amplitude of the out-of-phase voltages at the bases is inversely proportional to the frequency as a result of the series inductance in the feedback loop and the increasing input impedance of the transistors at low frequencies. Conversely, the negative feedback lowers the effective input impedance presented to the source (not the input impedance of the device itself) and with proper voltage slope would equalize it. With this technique, it is possible to maintain an input VSWR of 1.5:1 or less from 1.6 to 30 MHz.

### Impedance Matching and Transformers

Matching of the input and output impedances to 50 ohms, as well as the interstage matching, is accomplished with broadband transformers (Figures 3 and 4).

Normally only impedance ratios such as 1:1, 4:1, 9:1, etc., are possible with this technique, where the low impedance winding consists of metal tubes, through which an appropriate number of turns of wire is threaded to form the high-impedance winding. To improve the broadband characteristics, the winding inductance is increased with magnetic material. An advantage of this design is its suitability for large-quantity manufacturing, but it is difficult to find low-loss ferrites with sufficiently high permeabilities for applications where the physical size must be kept small



**Figure 3. Examples of broadband transformers.** Variations of these are used in all designs of this article (see text). All ferrites in transformers are Fair-Rite Products Corp. #2643006301 ferrite beads.\*

and impedance levels are relatively high. Problems were encountered especially with the output transformer design, where an inductance of 4  $\mu\text{H}$  minimum is required in the one-turn winding across the collectors, when the load impedance is

$$\frac{2(V_{CE} - V_{CEsat})^2}{P_{out}} = \frac{2(13.6 - 2.5)^2}{20} = 12.3 \text{ ohms}^{4,8}$$

Ferrites having sufficiently low-loss factors at 30 MHz range only up to 800 – 1000 in permeability and the inductance is limited to 2.5 – 3.0  $\mu\text{H}$  in the physical size required. This would also limit the operation to approximately 4 MHz, below which excessive harmonics are generated and the efficiency will degrade. One possible solution is to increase the number of turns, either by using the metal tubes for only part of the windings as in Figure 4B, or simply by winding the two sets of windings randomly through ferrite sleeves or a series of beads (Figures 3C and 4C). In the latter, the metal tubes can be disregarded or can be used only for mounting purposes. T3 was eventually replaced with a transformer of this type, although not shown in Figure 1.

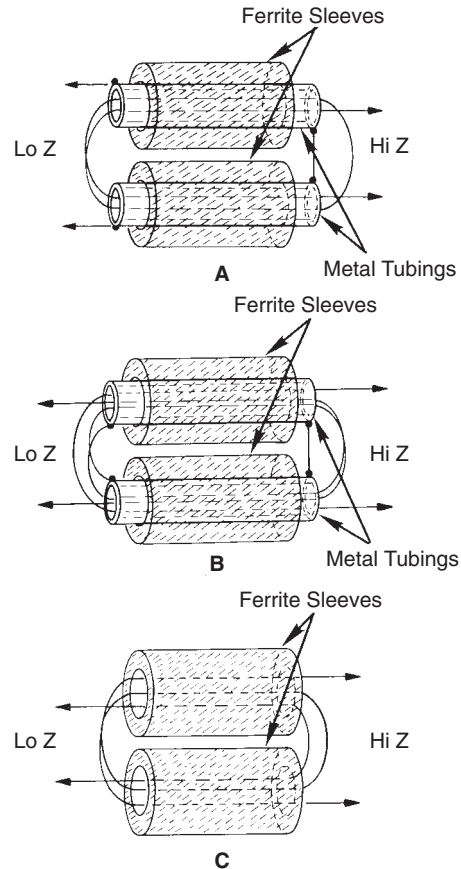
Below approximately 100 MHz, the input impedances of devices of the size of MRF475 and smaller are usually capacitive in reactance, and the  $X_s$  is much smaller than the  $R_s$ , (Low Q) For practical purposes, we can then use the formula

$$\sqrt{(R_s^2 + X_s^2)}$$

to find the actual input impedance of the device. The data-sheet numbers for 30 MHz are 4.5,  $-j2.4$  ohms, and we get

$$\sqrt{(4.5^2 + 2.4^2)} = 5.1 \text{ ohms.}$$

The base-to-base impedance in a push-pull circuit would be four times the base-to-emitter impedance of one transistor. However, in Class AB, where the base emitter junction is forward biased and the conduction angle is increased, the impedance becomes closer to twice that of one device. The rounded number of 11 ohms must then be matched to the



**Figure 4. The turns ratios shown above are imaginary and do not necessarily lead to correct design practices**

driver output. The drive power required with the 10 dB specified minimum gain is

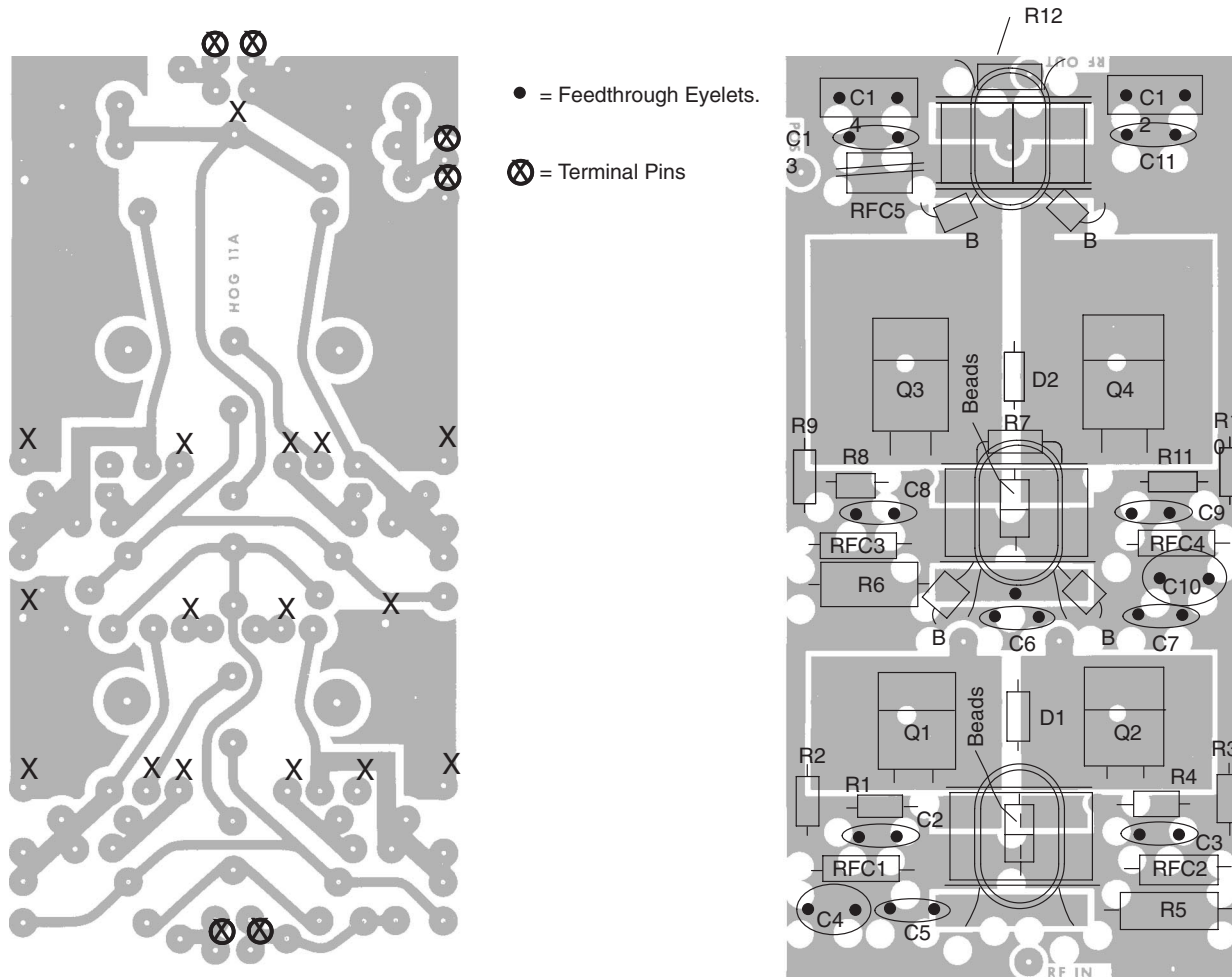
$$P_{out}/\text{Log}^{-1}(G_{PE}/10) = 2.0 \text{ W}$$

and the driver output impedance using the previous formula is  $2(11.1^2)/2 = 123$  ohms. The 11 ohms in series with the gain-leveling networks (C8, R8 and C9, R11) is 17 ohms. The closest practical transformer for this interface would be one with 9:1 impedance ratio. This would present a higher-than-calculated load impedance to the driver collectors, and for the best linearity the output load should be lower than required for the optimum gain and efficiency. Considering that the device input impedance increases at lower frequencies, a better overall match is possible with a 4:1, especially since the negative feedback is limited to only 4 dB at 2 MHz due to its effect on the efficiency and linearity.

The maximum amount of feedback a circuit can tolerate depends much on the physical layout, the parasitic inductances, and impedance levels, since they determine the phase errors in the loop. Thus, in general, the high-level stages should operate with lower feedback than the low-level stages.

The maximum amount of feedback the low-level driver can tolerate without noticeable deterioration in IMD is about 12 dB. This makes the total 16 dB, but from the data sheets we find that the combined gain variation for both devices from 2 to 30 MHz is around 29 dB. The difference, or 13 dB, should be handled by the gain-leveling networks.

\*Wallkill, N.Y. 12589



**Figure 5. Component Layout Diagram of Low-Cost 20 W Amplifier**

The leads of R7 and R12 form the one-turn feedback windings in T2 and T3. Ferrite beads in dc line can be seen located under T1 and T2.

The input impedance of the MRF476 is 7.55,  $-j0.65$  ohms at 30 MHz resulting in the base-to-base impedance of

$$2 \times \sqrt{(7.55^2 + 0.65^2)} = 15.2 \text{ ohms.}$$

This, in series with networks R1, C1 and R4, C3 (2 x 4.4 ohms), gives 24 ohms, and would require a 2:1 impedance ratio transformer for a 50-ohm interface. However, due to the influence of strong negative feedback in this stage, a better overall matching is possible with 4:1 ratio. The input networks were designed in a manner similar to that described in Reference 8.

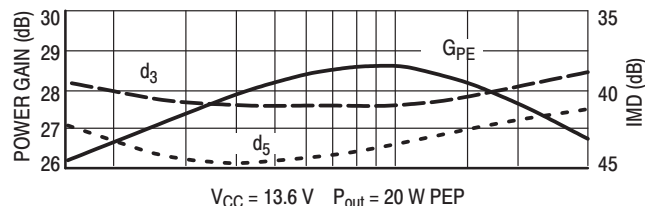
#### Measurements and Performance Data

At a power output of 20 W CW, all output harmonics were measured about 30 dB or more below the fundamental, except for the third harmonic which was only attenuated 17 dB to 18 dB at frequencies below 5 MHz. Typical numbers for the higher order distortion products (d9 and d11) are in the order of  $-60$  dB above 7 MHz and  $-50$  dB to  $-55$  dB at the lower frequencies. These both can be substantially reduced by increasing the idle currents, but larger heat sinks

would be necessary to accommodate the increased dissipation.

The efficiency shown in Figures 6 and 7 represents the overall figure for both stages. Currents through the bias networks, which are  $82/(13.6 - 0.7) = 0.16$  A each, are excluded. Modified values for R5 and R6 may have to be selected, depending on the forward voltage characteristics of D1 and D2.

Although this amplifier was designed to serve as a 1.6 to 30 MHz broadband driver, it is suitable for the citizens band use as well. With some modifications and design shortcuts, the optimization can be concentrated to one frequency.



**Figure 6. Intermodulation Distortion and Power Gain versus Frequency**



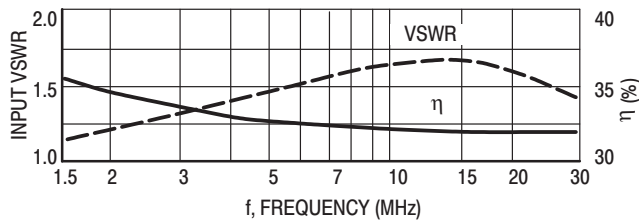


Figure 7. Input VSWR and Combined Collector Efficiency of Both Stages

## 20 W, 55 dB HIGH PERFORMANCE DRIVER

### 12-Volt Version

The second amplifier employs the MHW591 hybrid module to drive a pair of larger devices which can be operated Class A or AB, depending on the requirements. Transistors such as MRF449 and MRF455 are recommended for Class A and MRF433 for Class AB operation. A 24–28 volt version with MHW592 and a pair of MRF401s was also designed, and some of the test data will be presented. For Class A, the power parts should be replaced with MRF426s.\*

These amplifiers are a good example of how a good gain flatness can be achieved across the four-octave band, with simple RC input networks and negative feedback, while maintaining a reasonable input VSWR.

The MHW591 is employed as a predriver in this unit. The MHW591 and its counterpart, MHW592, were developed for low-level SSB driver applications from 1.0 MHz to 250 MHz. The Class A operation results in a steady-state current drain of approximately 0.32 A, which does not vary with the signal level. At an output level of 600 mW PEP, the IMD is typically better than –40 dB, which can be considered sufficiently good for most purposes. Since the power gain is specified as 36.5 dB, the maximum drive level for the 600 mW output is 0.13 mW, or –9 dBm. For the final power output of 20 W, a power gain of 15.2 dB minimum is required at the highest operating frequency for the power transistors. A good, inexpensive device for this is the MRF433, which has a 20 dB minimum gain and –30 dB IMD specification at an output level of 12.5 W PEP. The push-pull configuration, due to inconsistent ground planes and broadbanding due to matching compromises usually results in 2 dB to 3 dB gain losses from figures measured in a test fixture. Assuming a transistor power gain of 18 dB, the total will be 54.5 dB, representing an input power of –11 dBm. Later measurements, however, indicated a gain of 56 dB ( $\pm 0.5$  dB) at the specified power output, making the input level around –13 dBm.

### Biasing and Feedback

The bias circuit employed with this amplifier is basically similar to the one described earlier, with the exception of having an emitter follower output. A second diode in series with the one normally seen with the clamping diode method compensates for the voltage drop in the base-emitter junction of the emitter follower, Q1 (Figure 8). The minimum current through D1 and D2 is  $(I_C/h_{FE})(Q2 + Q3)/h_{FE}(Q1)$ ,

and in this case  $(2.5/40)/40 = 1.5$  mA. Typical  $h_{FE}$  for the MRF433 is 40, and with the devices biased to 200 mA each, the standby base current is 10 mA. In operation the load current of Q1 then varies between 10 and 62 mA. A Case 77 transistor exhibiting low variations in base-emitter saturation voltage over this current range is MJE240. Base-emitter saturation voltage determines the bias source impedance, which should not exceed approximately 0.3 ohm, representing a 20 mV variation in voltage from idle to full drive conditions. If source impedance exceeds 0.3 ohms, a capacitor of 500–1000  $\mu$ F should be connected from the emitter of Q1 to ground.

The peak dissipation of Q2 is under one watt, making it possible to mount the transistor directly to the circuit board without requiring any additional heat sinking.

Diodes D1 and D2 are located on the lower side of the board, near Q2 and Q3 (Figure 9). The leads are formed to allow the diodes to come into contact with the transistor flanges. The thermal contact achieved in this manner is not the best possible, even when the gaps are filled with silicone compound, but the thermal time constant is lower than with most other methods. Both diodes are used for temperature tracking, although the voltage drop of only one is required to compensate for the  $V_{BE}$  forward drop of Q1. The advantages of this circuit are simplicity, low standby current drain, and ease of adjustment with a small trimpot.

The voltages for the negative feedback are derived separately from the collectors of Q2 and Q3 through L6, R6 and L7, R7. Capacitors C5 and C6 are used for dc isolation. Because of the high RF voltage levels on the collectors, this method is only feasible in low- and medium-power amplifiers. At higher power levels, the power-handling requirements for the series resistors (Figure 8), which must be noninductive, become impractical. A feedback voltage source with lower impedance must be provided in such cases.<sup>8</sup>

The MRF433 has a higher figure of merit (emitter periphery/base area) than the MRF475, for example. This results in smaller differences in power gain per given bandwidth, since the device is operating farther away from the 6 dB/octave slope.<sup>9</sup> Disregarding the package inductances, which affect the Q, the higher figure of merit makes such devices more suitable for broadband operation. The 2 MHz and 30 MHz  $\Delta G_{PE}$  of the MRF433 is 8 dB, which is divided equally between the negative feedback and the leveling networks C3, R4 and C4, R5. The 2 MHz and 30 MHz impedance values are 9.1, –j3.5 and 2.5, –j2.2 ohms, respectively, although the 2 MHz values are not given in the data sheet.

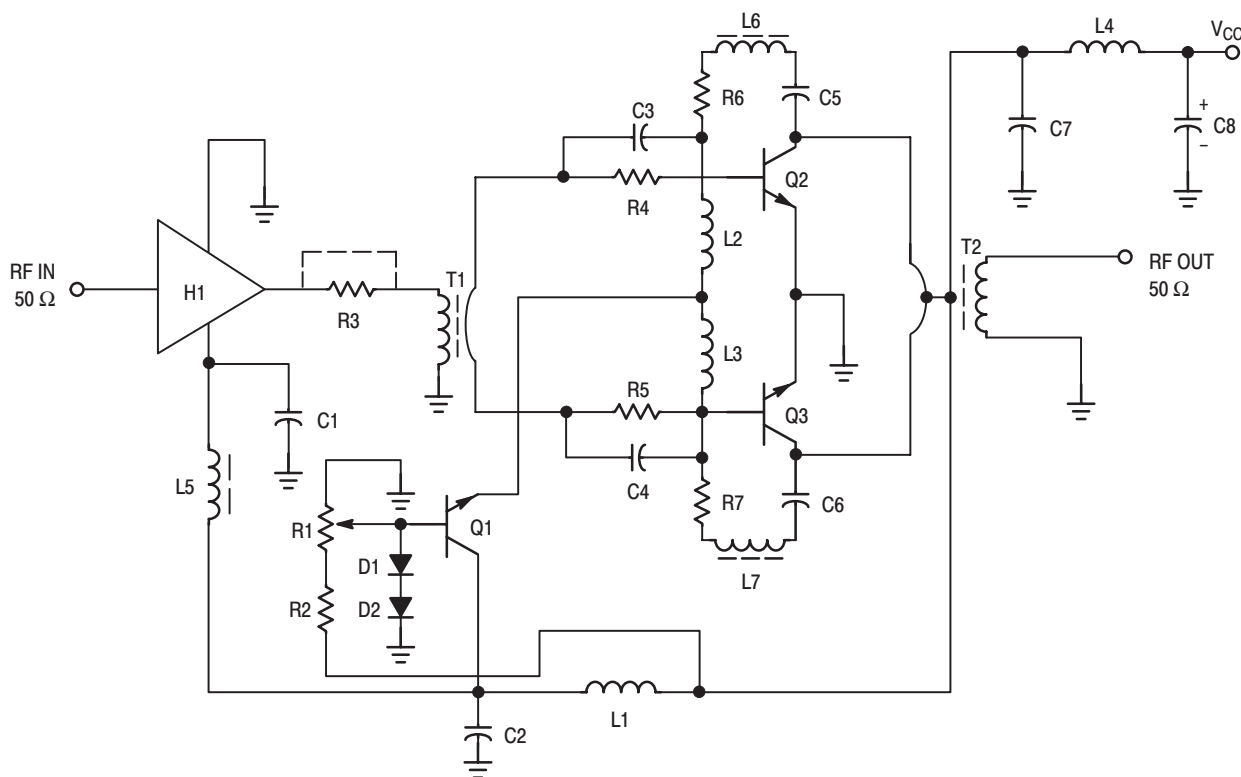
At 30 MHz we can first determine what type of transformer is needed for the 50-ohm input interface. The effective transformer load impedance is  $2\sqrt{(2.5^2 + 2.2^2)} + 2$  (2.4) ohms (leveling networks) = 11.5 ohms, which indicates that 4:1 impedance ratio is the closest possible (see Figures 3B, 4A, and 8). These values are accurate for practical purposes, but they are not exact, since part of the capacitive reactance in C3 and C4 will be cancelled, depending on the transformer characteristics.

\*To be introduced.

## 28-Volt Version

six turns of RG-196 coaxial cable wound on an Indiana General F-627-8-Q1 toroid. Each end of the braid is connected to the collectors, and the inner conductor forms the secondary. A connection is made in the center of the braid (three turns from each end) to form the center tap and dc feed.

In designing the gain-leveling networks, another approach can be taken, which does not involve the computer program described in Reference 8. Although the input VSWR is not optimized, it has proved to give satisfactory results.



- R1 — 1 k Trimpot  
R2 — 1 k Ohm, 1/4 W  
R3 — Optional  
R4, R5 — 5, 6 Ohms, 1/4 W  
R6, R7 — 47 Ohms, 1/4 W  
C1, C2, C5, C6, C7 — 0.01  $\mu$ F Chip  
C3, C4 — 1800 pF Chip  
C8 — 10  $\mu$ F/35 V Electrolytic

- L1, L4, L5 — Ferrite Beads (Fair-Rite Products Corp.  
#2643000101 or Ferroxcube #56 590 65/3B or equivalent)  
L2, L3 — 10  $\mu$ H Molded Choke  
L6, L7 — 0.1  $\mu$ H Molded Choke  
Q1 — MJE240  
Q2, Q3 — MRF433  
H1 — MHW591  
T1, T2 — 4:1 and 1:4 Impedance Transformers, respectively.  
(See discussion on transformers.) Ferrite Beads are  
Fair-Rite #2643006301 or equivalent)

### Figure 8. Schematic and Components Parts list

\* NOTE: Parts and kits for this amplifier are available from Communication Concepts Inc., 508 Millstone Drive, Beavercreek, Ohio 45434-5840 (513) 426-8600.

The amount of negative feedback is difficult to determine, as it depends on the device type and size and the physical circuit layout. The operating voltage has a minimal effect on the transistor input characteristics, which are more determined by the electrical size of the die. High-power transistors have lower input impedances and higher capacitances, and phase errors are more likely to occur due to circuit inductances.

Since the input capacitance is an indication of electrical size of the device, we can take the paralleled value ( $X_p$ ) at 2 MHz, which is  $X_s + (R_s^2 / X_s)$  and for MRF433  $3.5 + (9.1^2 / 3.5) = 27$  ohms. The  $X_p$  of the largest devices available today is around 10 ohms at 30 MHz, and experience has shown that the maximum feedback should be limited to about 5 dB in such case. Using these figures as constants, and assuming the  $G_{PE}$  is at least 10 dB, we can estimate the amount of feedback as:  $5 / (10^2 / 27) + 5 = 6.35$  dB, although only 4 dB was necessary in this design due to the low  $\Delta G_{PE}$  of the devices.

The series base resistors ( $R_4$  and  $R_5$ ) can be calculated for 4 dB loss as follows:

$$\frac{[(V_{in} \times \Delta 4 \text{ dB}) - V_{in}]}{I_{in}} = \frac{[(0.79 \times 1.58) - 0.79]}{0.04}$$

$$= 11.45 \text{ ohms, or}$$

$$11.45/2 = 5.72 \text{ ohms each.}$$

$$Z_{in} (2 \text{ MHz}) = \sqrt{(9.1^2 + 3.5^2)} = 9.75 \text{ ohms,}$$

in Class AB push-pull 19.5 ohms.

$$P_{in} = 20 \text{ W} - 28 \text{ dB} = 20/630 = 0.032 \text{ W}$$

$$V_{RMS} (\text{base to base}) = \sqrt{(0.032 \times 19.5)} = 0.79 \text{ V}$$

$$I_{in} = V_{in}/R_{in} = 0.79/19.5 = 0.04 \text{ A}$$

$$\Delta V 4 \text{ dB} = \sqrt{[\text{Log}^{-1} (4/10)]} = 1.58 \text{ V}$$

The parallel capacitors ( $C_3$  and  $C_4$ ) should be selected to resonate with  $R$  (5.7 ohms) somewhere in the midband. At 15 MHz, out of the standard values, 1800 pF appears to be the closest, having a negligible reactance at 2 MHz, and 2.8 ohms at 30 MHz, where most of the capacitive reactance is canceled by the transformer winding inductance.

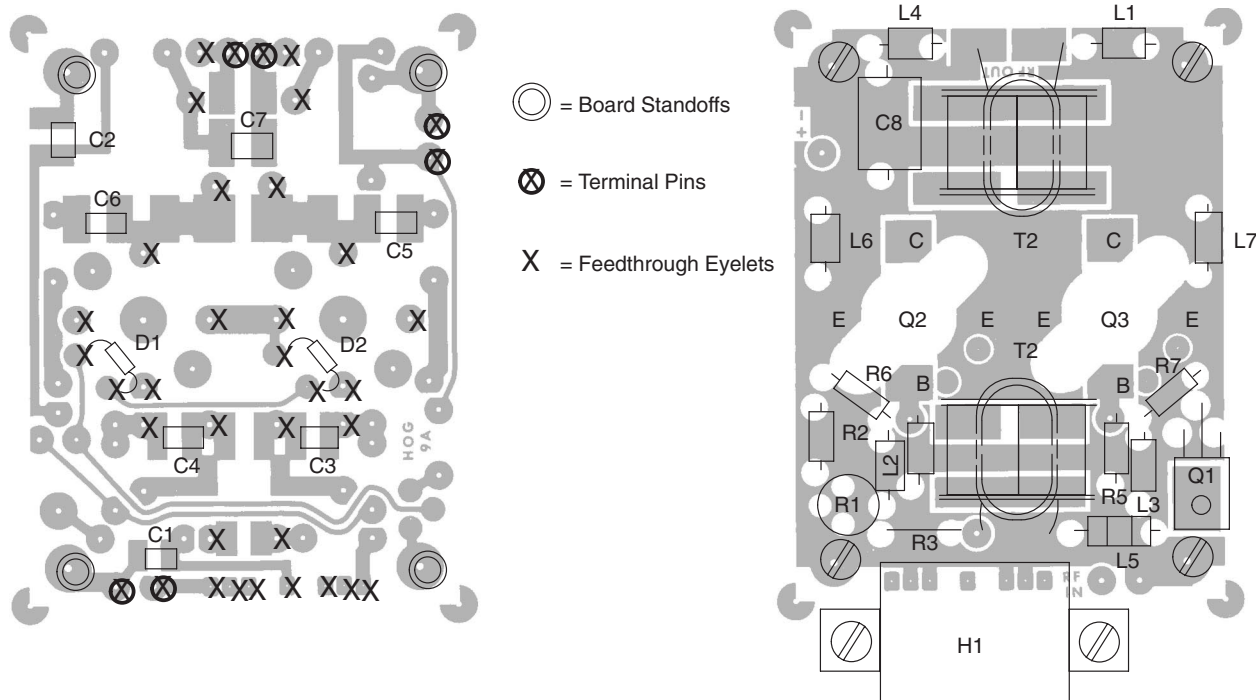


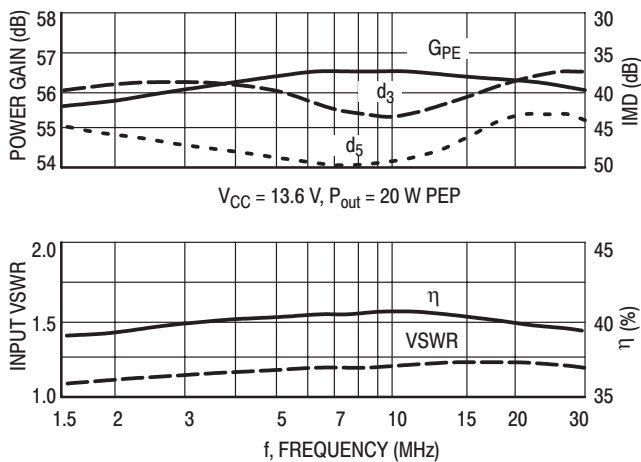
Figure 9. Component Layout Diagram of 20 W, 55 dB High-Performance Drive

The leads of  $D_1$  and  $D_2$  are bent to allow the diodes to contact the transistor mounting flanges.

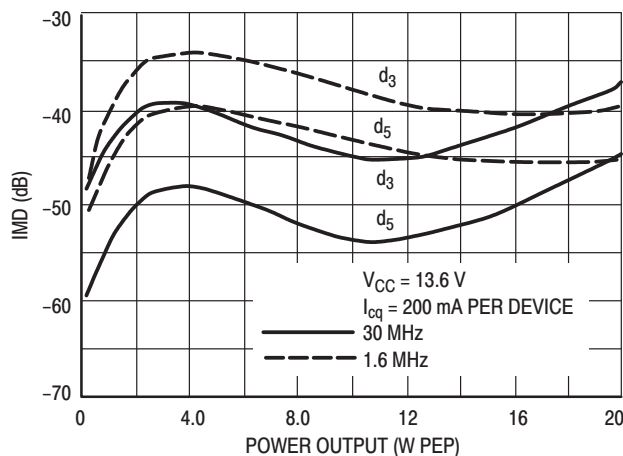
Note: The mounting pad of  $Q_1$  must be connected to the lower side of the board through an eyelet or a plated through-hole.

## Measurements and Performance Data

The output harmonic contents of this amplifier are substantially lower than normally seen in a Class AB system operating at this power level and having a 4.5 octave bandwidth. All harmonics except the third are attenuated more than 30 dB across the band. Between 20 and 30 MHz, – 40 to – 55 dB is typical. The third harmonic has its highest amplitude (– 20 to – 22 dB), as can be expected, below 20 MHz. The measurements were done at an output level of 20 W CW and with 200 mA collector idle current per device. Increasing it to 400 mA improves these numbers by 3–4 dB, and also reduces the amplitudes of  $d_5$ ,  $d_7$ ,  $d_9$ , and  $d_{11}$  by an average of 10 dB, but at the cost of 2–3 dB higher  $d_3$ .



**Figure 10. Intermodulation Distortion and Power Gain versus Frequency (Upper Curves). Input VSWR and Collector Efficiency (excluding MHW591) (Lower Curves).**



**Figure 11. IMD versus Power Output**

## CONCLUSION

The stability of both designs (excluding the 28 V unit) was tested into reactive loads using a setup described in Reference 8. Both were found to be stable into 5:1 load mismatch up to 7 MHz, 10:1 up to 30 MHz, except the latter design did not exhibit breakups even at 30:1 in the 20 – 30 MHz range. If the test is performed under two-tone conditions, where the power output varies from zero to maximum at the rate of the frequency difference, it is easy to see at once if instabilities occur at any power level.

The two-tone source employed in all tests consists of a pair of crystal oscillators, separated by 1 kHz, at each test frequency. The IMD ( $d_3$ ) is typically – 60 dB and the harmonics – 70 dB when one oscillator is disconnected for CW measurements.

HP435 power meters were used with Anzac CH-130-4 and CD-920-4 directional couplers and appropriate attenuators. Other instruments included HP141T analyzer system and Tektronix 7704A oscilloscope-spectrum analyzer combination.

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The PCB layouts below are a supplement to Figures 5 and 9 and may be used for generating printed circuit artwork.  
NOTE: Not to scale.

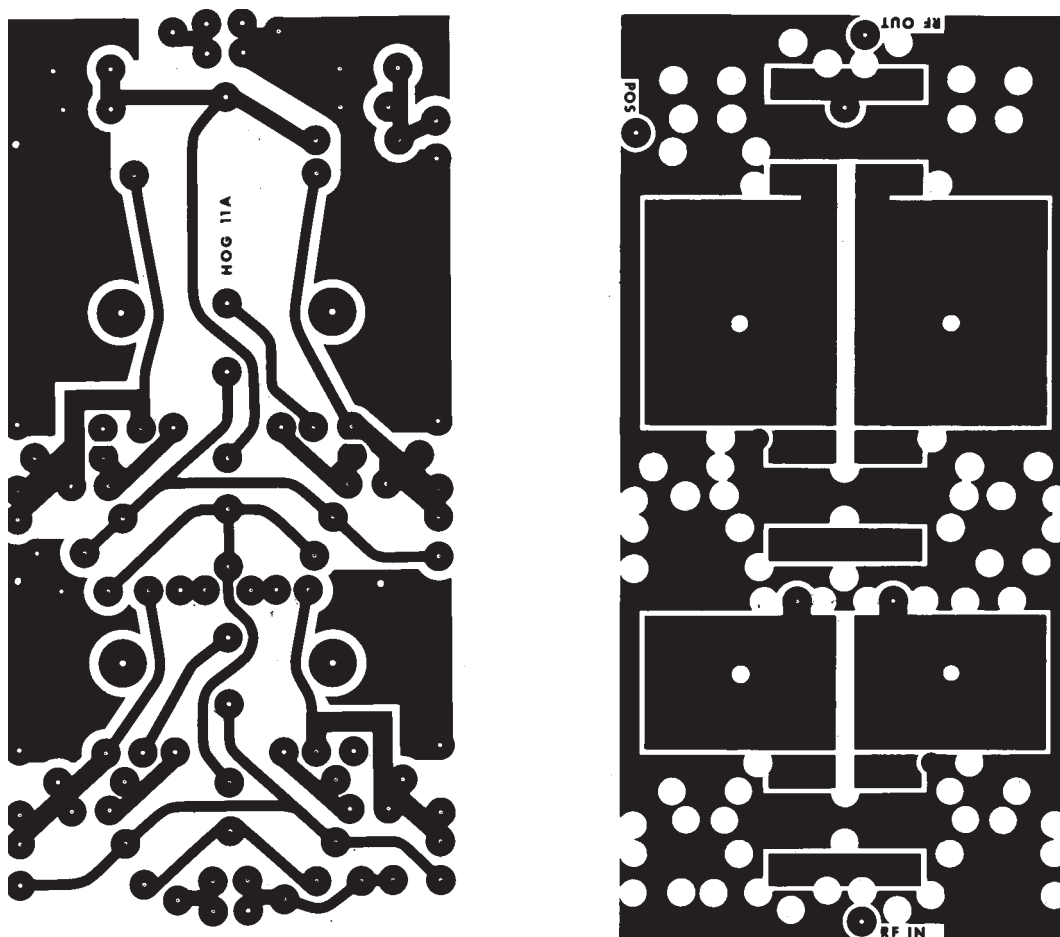


Figure 12. Layout of Low-Cost 20 W Amplifier

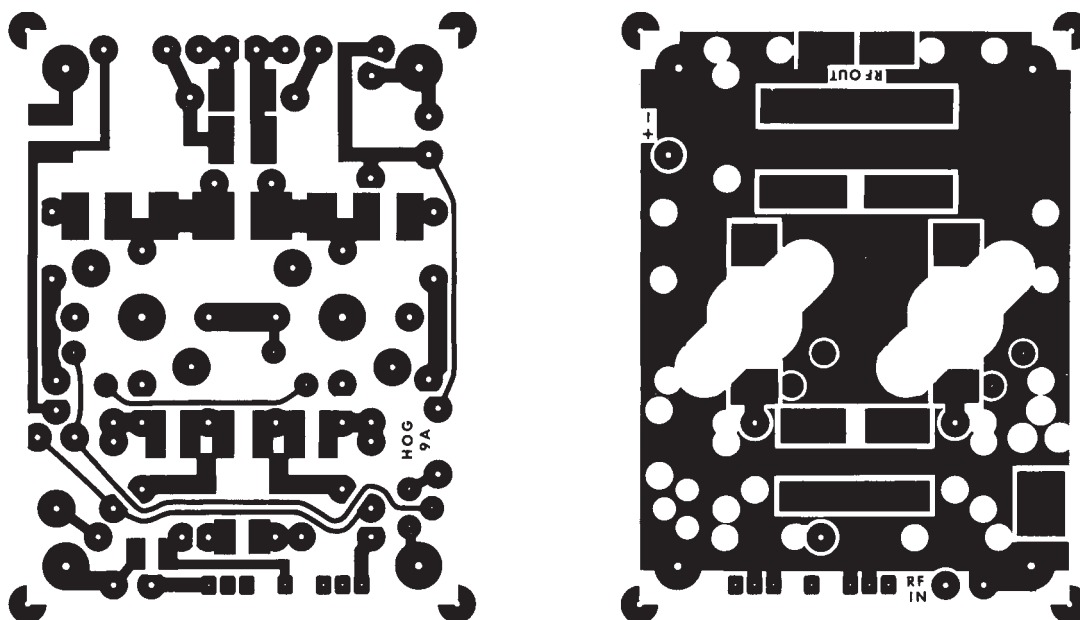


Figure 13. PCB Layout of 20 W, 55 dB High-Performance Driver

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JAPAN: Nippon Motorola Ltd.; 4-32-1, Nishi-Gotanda, Shinagawa-ku, Tokyo 141, Japan.

ASIA PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Center, No. 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong.


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