

# Bias Circuits for RF Devices

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A lot of RF schematics mention: “bias circuit not shown”; when actually one of the most critical yet often overlooked aspects in any RF circuit design is the bias network.

The bias network determines the amplifier performance over temperature as well as RF drive. The DC bias condition of the RF transistors is usually established independently of the RF design. Power efficiency, stability, noise, thermal runaway, and ease to use are the main concerns when selecting a bias configuration.

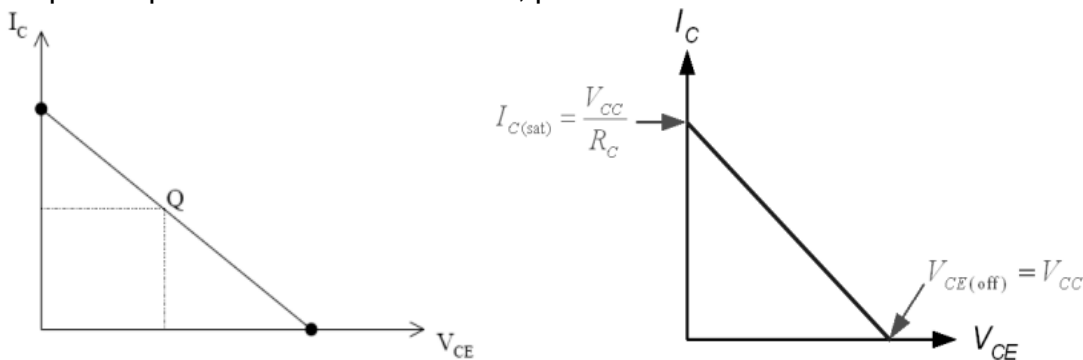
A transistor amplifier must possess a DC biasing circuit for a couple of reasons.

- We would require two separate voltage supplies to furnish the desired class of bias for both the emitter-collector and the emitter-base voltages.
- This is in fact still done in certain applications, but biasing was invented so that these separate voltages could be obtained from but a single supply.
- Transistors are remarkably temperature sensitive, inviting a condition called thermal runaway. Thermal runaway will rapidly destroy a bipolar transistor, as collector current quickly and uncontrollably increases to damaging levels as the temperature rises, unless the amplifier is temperature stabilized to nullify this effect.

## Amplifier Bias Classes of Operation

Special classes of amplifier bias levels are utilized to achieve different objectives, each with its own distinct advantages and disadvantages. The most prevalent classes of bias operation are Class A, AB, B, and C. All of these classes use circuit components to bias the transistor at a different DC operating current, or “ $I_{CQ}$ ”.

When a BJT does not have an A.C. input, it will have specific D.C. values of  $I_C$  and  $V_{CE}$ . These values will correspond to a specific point on the D.C. load line, point named Quiescent Current  $I_{CQ}$ .



In the graph above the circuit is said to be midpoint biased since the values of  $I_C$  and  $V_{CE}$  at Quiescent-point are one-half of their maximum values.

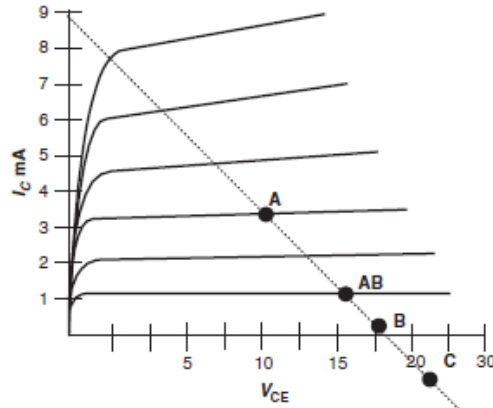
**Class A** single-ended amplifiers are ordinarily used only in small-signal non-power applications. Class A will generally require a constant current bias source to fix the operating point regardless of the RF drive and output. The circuit will have to have some sort of feedback to keep the output current at a fixed level, or a circuit must be created whose current is large compared to the amount of output power required (i.e., it is quasi class A in that the operating point movement is minimal).

Simply by decreasing the  $I_{CQ}$  of the amplifier by a small amount, **Class AB** operation can be reached.

But any Class AB single-ended power amplifier will create more output distortion than a Class-A type due the output clipping of the signal's waveform.

Class AB or B operations require some form of positive biasing - though the operating point will move with RF drive. This will require an “open loop” circuit with some sort of compensation over ambient conditions.

**Class C** will generally require a negative bias of some kind—or in most cases, the input of the transistor is tied to ground with an inductor or resistor, which is sufficient to keep the conduction angle correct.



Typical BJT Load-Line Characteristic for Different Bias Classes

The most predominant biasing schemes used to obtain both temperature stabilization and single-supply operations are:

- base-biased emitter feedback
- voltage-divider emitter feedback
- collector-feedback
- diode feedback
- active-feedback bias

All five are found in Class A and AB operation, while Class B and C amplifiers can implement other methods.

### Biasing Considerations for RF Bipolar Junction Transistors (BJT)

Usually the manufacturer supplies in their datasheets a curve showing  $f_t$  versus collector current for a bipolar transistor.

- For good gain characteristics, it is necessary to bias the transistor at a collector current that results in maximum or near-maximum  $f_t$ .
- On the other hand, for best noise characteristics, a low current is generally most desirable.

Finally, one must consider the maximum signal level expected at the input of the transistor.

- The bias point must be at a sufficiently high current (and voltage) level to prevent the input signal from swinging the collector current out of the “linear” region of operation. It is assumed that a transistor has been chosen having a sufficient operating current level to prevent the input signal from driving the transistor into the so-called saturated region of operation, which would also be an operating condition that would prevent linear operation.
- If the amplifier is to work over a range of temperature, have to design a bias network that maintains the D.C. bias point as the operating temperature changes.

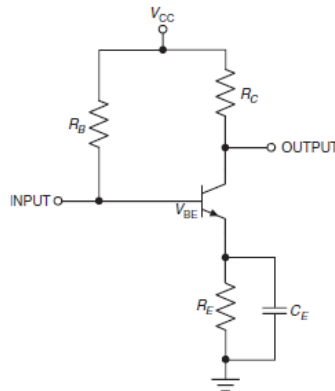
Two basic internal transistor characteristics are known to have a significant effect on the DC bias point. These are  $\Delta V_{BE}$  and  $\Delta \beta$ .

- The base-emitter voltage of a bipolar transistor decreases with increasing temperature at the rate of about 2.5 mV/°C. Emitter voltage  $V_E$  tends to minimize the effect because as base current increases (as  $V_{BE}$  decreases), collector current increases, and this causes  $V_E$  to increase also. However, as  $V_E$  increases, collector current tends to decrease.
- In the same time, the transistor’s D.C. current gain  $\beta$  typically increases with increasing temperature at the rate of about 0.5% per degree Celsius.

The BJT is quite often used as a Low Noise Amplifier due to its low cost. With a minimal number of external matching networks, the BJT can quite often produce an LNA with RF performance considerably better than an MMIC. Of equal importance is the DC performance. Although the device's RF performance may be quite closely controlled, the variation in device DC parameters can be quite significant due to normal process variations.

- Important for an RF BJT is that variation in  $h_{FE}$  from device to device (up to 3 to 1) will generally not show up as a difference in RF performance.
- Two BJT devices with widely different  $h_{FE}$ 's can have similar RF performance as long as the devices are biased at the same  $V_{CE}$  and  $I_C$ . This is the primary purpose of the bias network, i.e., to keep  $V_{CE}$  and  $I_C$  constant as the DC parameters vary from device to device.

**Base-biased emitter feedback** works in the following way: The base resistor ( $R_B$ ), the 0.7 V base-to-emitter voltage drop ( $V_{BE}$ ), and the emitter resistor ( $R_E$ ), are all in series;



Base-biased emitter feedback

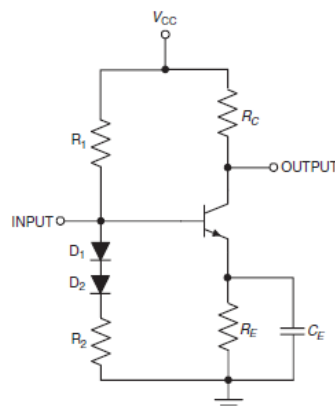
- As the collector current ( $I_C$ ) increases due to a rise in the transistor's temperature, the current through the emitter resistor will also increase, which increases the voltage dropped across  $R_E$ .
- This action lowers the voltage that would normally be dropped across the base resistor and, since the voltage drops around a closed loop must always equal the voltage rises, this reduction in voltage across  $R_B$  decreases the base current, which then lowers the collector current.

The capacitor ( $C_E$ ) located across  $R_E$  bypasses the RF signal around the emitter resistor to stop excessive RF gain degeneration in this circuit.

The higher the voltage across  $R_E$  ( $V_E$ ), the more temperature stable the amplifier, but the more power will be wasted in  $R_E$  due to  $V_E^2/R_E$ , as well as the decreased AC signal gain if  $R_E$  is not bypassed by a low reactance capacitor.

Standard values of  $V_E$  for most HF (high frequency, or amateur band) designs are between 2 to 4 V to stabilize  $\Delta V_{BE}$ . UHF amplifiers and higher frequencies will normally completely avoid these emitter resistors.

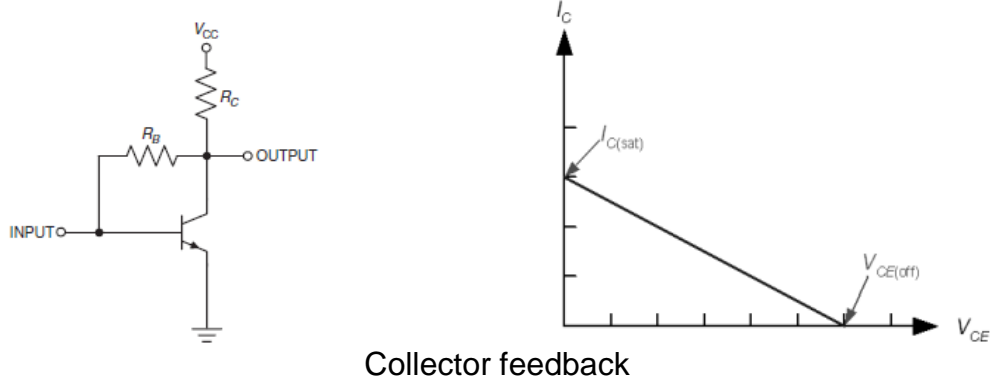
For better temperature compensation the most common method is **Diode Temperature Compensation**. Two diodes, D1 and D2, attached to the transistor's heatsink or to the device itself, will carefully track the transistor's internal temperature changes.



Diode temperature compensation bias

This is accomplished by the diode's own decrease in its internal resistance with any increase in heat, which reduces the diode's forward voltage drop, thus lowering the transistor's base-emitter voltage, and diminishing any temperature-induced current increase in the BJT.

A very low-cost biasing scheme for RF and microwave circuits, but with less thermal stability than above, is called **collector-feedback bias**.



The circuit, employs only two resistors, along with the active device, and has very little lead inductance due to the emitter's direct connection to ground.

Collector-feedback bias temperature stabilization functions so:

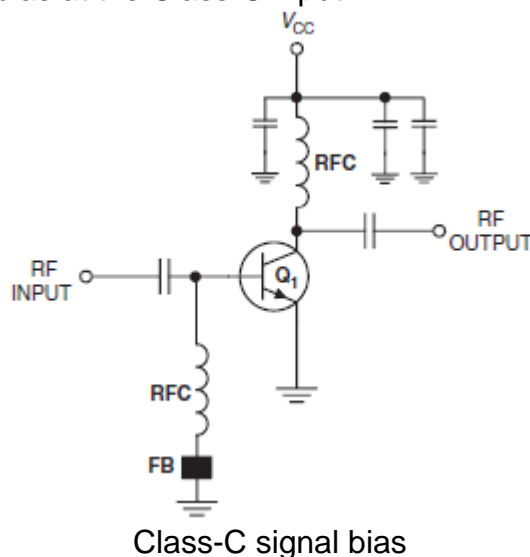
- As the temperature increases, the transistor will start to conduct more current from the emitter to the collector.
- But the base resistor is directly connected to the transistor's collector, and not to the top of the collector resistor as in the above biasing techniques, so any rise in  $I_C$  permits more voltage to be dropped across the collector resistor.
- This force less voltage to be dropped across the base resistor, which decreases the base current and, consequently,  $I_C$ .

For bipolar transistors, Class-C amplifiers permit the use of three biasing techniques:

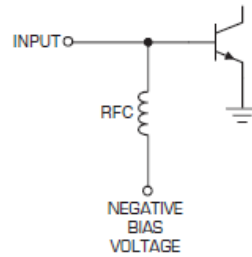
- signal
- external
- self bias

The average Class-C transistor amplifier is normally not given any bias at the base whatsoever, but in order to lower the chances of any BJT power device instability the base should be grounded through a low-Q choke, with a ferrite bead on the base lead's grounded end.

These biasing techniques will still require an RF signal with high enough amplitude to overcome the reverse (or complete lack of) bias at the Class-C input.



A less common method in Class-C amplifiers is to use an **external bias**.

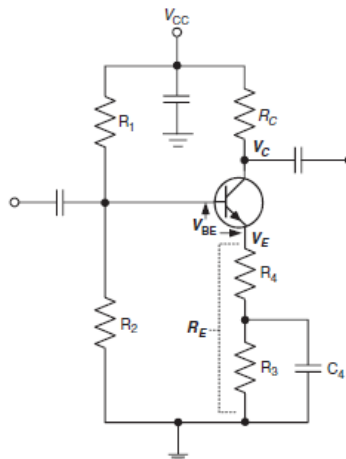


Class-C external bias

This circuit uses a negative bias supply to bias the base, and a standard positive supply for the collector circuit. The RFC acts as high impedance for the RF frequency itself so that it does not enter the bias supply.

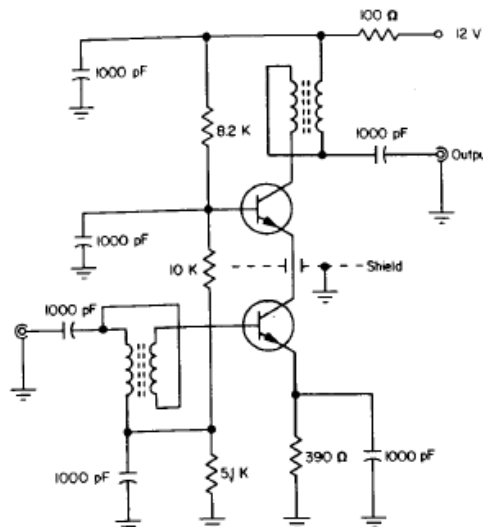
Some low-frequency high gain IF amplifiers (Intermediate Frequency) will split the single emitter feedback resistor into two separate emitter resistors, with only one of these resistors having an AC capacitor bypass, while the other one is providing constant degenerative feedback to enhance amplifier stability, reducing the chance of oscillations.

This topology allows to solidly setting the gain of the amplifier, just changing the value of  $R_4$  resistor.



Stable IF Amplifier

Cascode approach is a configuration that is inherently stable. In the example below the first transistor operates common emitter and sees as its load, the low input impedance of a common base stage. The 10k base resistor is common for both stages, and the bias is done through a 2:1 transformer used to get a wide-band matching.



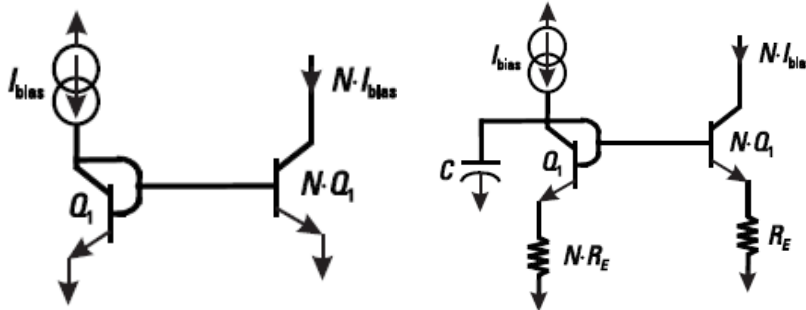
Stable BJT Cascode LNA with resistive bias scheme

## Highly Stable Active Bias for High Frequency BJT Amplifiers

The most common form of biasing in RF circuits is the current mirror. This basic stage is used everywhere and it acts like a current source. It takes a current as an input and this current is usually generated, along with all other references, by a circuit called a bandgap reference generator.

- A bandgap reference generator is a temperature-independent bias generating circuit.
- The bandgap reference generator balances the  $V_{BE}$  dependence on temperature, to result in a voltage or current nearly independent of temperature.

The most basic current mirror topologies are:



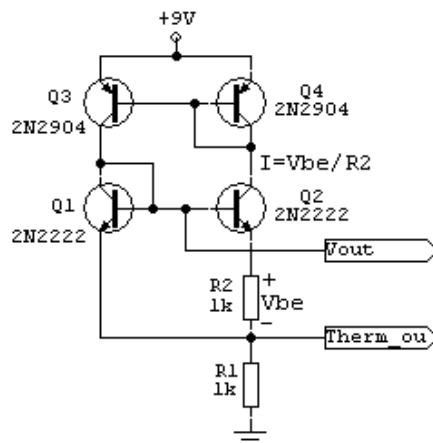
In this mirror, the bandgap reference generator produces current  $I_{bias}$  and forces this current through  $Q_1$ . Scaling the second transistor allows the current to be multiplied up and used to bias working transistors.

- One major drawback to this circuit is that it can inject a lot of noise at the output due primarily to the gain of the transistor  $Q_1$  which acts like an amplifier for noise.
- A capacitor can be used to clean up the noise, and resistors degeneration can be put into the circuit to reduce the gain of the transistor.
- With any of mirror topologies, a voltage at the collector of  $N.Q_1$  must be maintained above a minimum level or else the transistor will go into saturation. Saturation will lead to bad matching and nonlinearity.

### Temperature Reference Circuits

- The general recipe for making temperature independent references is to add a voltage that goes up with temperature to one that goes down with temperature.
- If the two slopes cancel, the sum will be independent of temperature.

To realize this idea bandgap voltage reference circuits are the most used. It produces an output voltage that is traceable to fundamental constants and therefore relatively insensitive to circuit variations, temperature and supply.



Temperature reference circuit

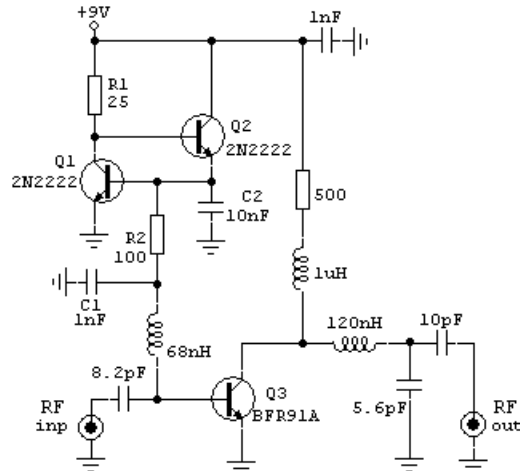
With proper choice of  $R_1$  and  $R_2$ , the output voltage will have zero variation with temperature, providing in the same time at the emitters of  $Q_1$  and  $Q_2$  a voltage proportional with temperature (thermometer output).

Generally, it is stated that the output impedance of the bias circuitry should be kept small, in order to increase the linearity of the output bias stage.

However, the output impedance is typically designed to have a large resistance in order to reduce the noise contribution from the bias circuitry, and to avoid significant loading on the RF input port.

For example, to use an inductor in the bias circuit to form low impedance near DC, and high impedance near the RF signal band.

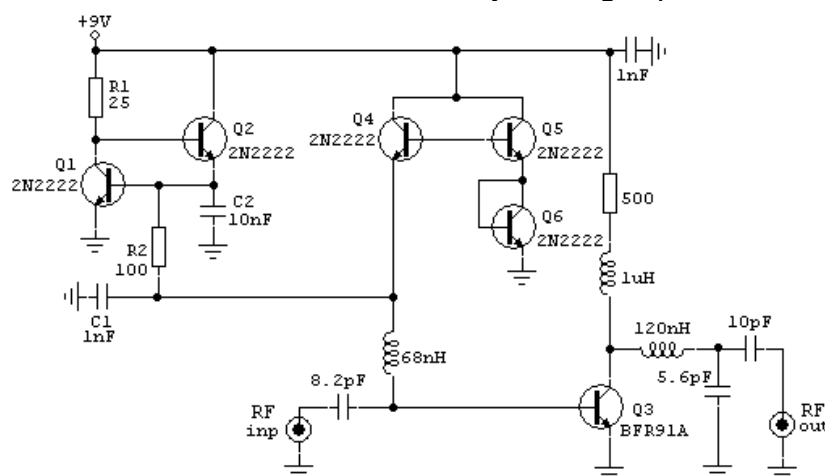
- It is difficult to compare different bipolar LNA's if the biasing arrangement is not mentioned.
- Using an external bias from an external power supply can increase the IIP3 of an LNA compared to an LNA with an on-chip bias.



Active bias LNA

- The transistor, Q2, increases the accuracy of the current mirror, since the required base current for the LNA and Q1 is not taken from the reference current,  $I_{R1}$ .
- It may be necessary to remove Q2 for low supply voltages, since the current mirror formed by LNA, Q1, and Q2 requires a supply which is at least two times the base emitter voltage.
- Sometimes high-frequency LNA's use an emitter degeneration inductor for better matching, and is possible that the series resistance of this inductor to affect the accuracy of the current mirror.
- The NF of the LNA is increased if the noise from the bias is not properly filtered out. This can be done by using appropriate filtering capacitors. This can be done by using appropriate filtering capacitors as C1 and C2, which shunt the noise from the biasing to ground.
- If Q3 is a power amplifier mounted on a heatsink, Q2 shall be mounted on its own heatsink for power dissipation, when Q1 shall be mounted on the main heatsink, as close as possible to the RF transistor, in order to perform temperature compensation.

A different method used to increase the IIP3 of the LNA by biasing is presented below:

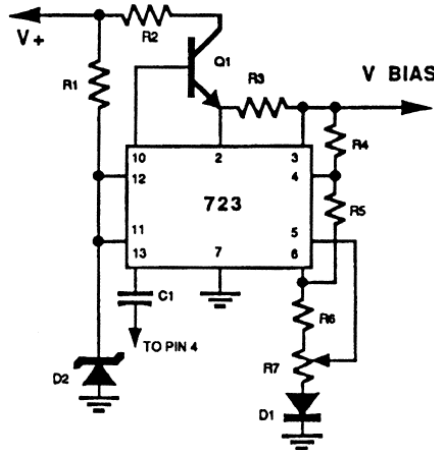


Dual-bias LNA

The dual-biasing is constructed using two different bias paths. The primary biasing is a current mirror and the secondary bias a diode bias feed circuit.

- With a small signal, the current mirror provides the bias current for the Q3 LNA.
  - When the signal is increased, the Q3 base current increases and the voltage across the biasing resistor R2 increases, reducing the base voltage.
  - As the voltage drops, the current to the base of the input transistor through the diode bias-feed (Q4) increases, compensating the base-voltage drop.
  - Therefore, the LNA linearity and compression point are both improved.
  - This bias circuit features the lowest source impedance of the less complex bias circuits.
- Therefore, it is recommended for high power device biasing and for other demanding applications.

### Bias Circuit using supply regulator



The main advantages of the bias source shown in the figure above:

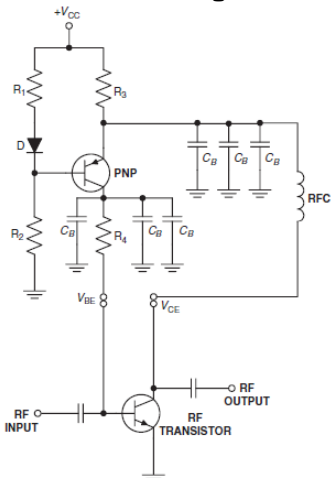
- The circuit it provides the lowest source impedance at a relatively low cost,
- The bias voltage remains independent of variations in the power supply voltage
- Temperature compensation is easy to implement.

The diode D1 performs this function and should be in thermal contact with the heat source.

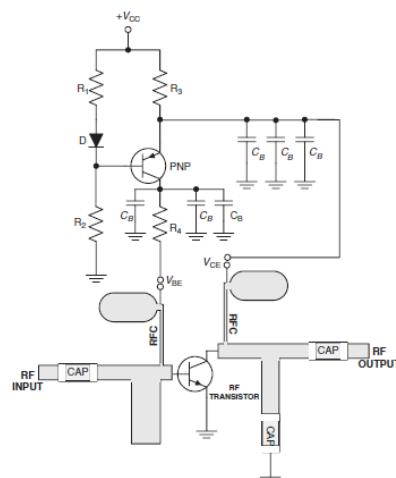
Depending on the current requirement and the pass transistor used, Q1 may have to be cooled. It has a positive temperature coefficient to the bias voltage, but the temperature coefficient is negligible compared to the negative coefficient of D1. This permits Q1 to be attached to the main heat sink. R1 and D2 are only necessary if the RF amplifier is operated at a supply voltage higher than 40 V, which is the maximum rating for the regulator.

This circuit also provides regulation against supply variations. The source impedance mainly depends on the  $h_{FE}$  of Q1.

### Active bias design for LNA's using lumped elements or distributed elements.



Active-bias LNA – Lumped elements



Active-bias LNA – Distributed elements



- The bias circuit shown has to be carefully bypassed at both high and low frequencies.
- There is one inversion from base to collector of RF transistor, and another inversion may be introduced by RFC, matching components and stray capacitances, resulting in positive feedback around the loop at low frequencies.
- Low ESR electrolytic or tantalum capacitor from the collector of Q2 to ground is usually adequate to ensure stability.

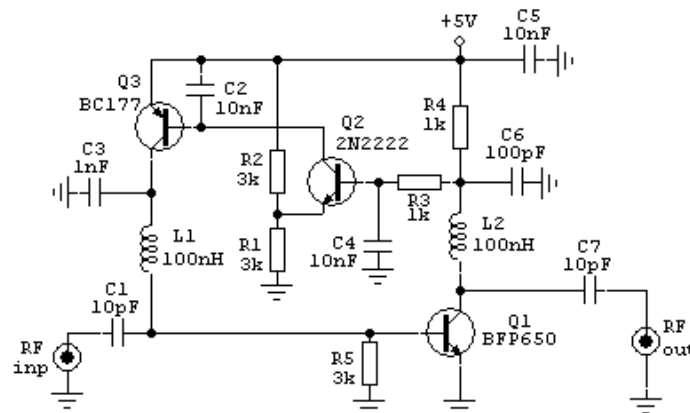
Steps designing an active bias for the schematic above:

1. Select an  $I_D$  current through the diode of 2 mA.
2. Select an appropriate  $I_C$  current for Class-A bias of the RF transistor amplifier
3. Select a  $V_{CC}$  for the active bias network that is approximately 2V or 3V greater than the  $V_{CE}$  required for the RF transistor.
4. Select an RF choke (RFC) for the active bias circuit with the appropriate SRF (self resonant frequency) that is greater than the frequency of operation.
5. Select both a silicon PNP transistor with a beta of at least 30 and a low-frequency silicon diode (a PNP transistor is used so that the  $V_{CC}$  may be a positive voltage)

- The idea adding a diode in the circuit is to compensate for the  $-2.5 \text{ mV}/^\circ\text{C}$  of the PNP base-emitter junction with the same factor introduced appropriately into the active bias circuit.

### Active Voltage-Feedback Bias

A good biasing scheme is shown below and uses two transistors (PNP and NPN) in a voltage-feedback scheme from the collector to the base of Q1.



Voltage-Feedback Bias

- The voltage-feedback it maintains the collector of the RF LNA Q1 at one-half the supply voltage plus one  $V_{BE}$  (base-to-emitter voltage, about 0.4V).
- Transistor Q2 measures the voltage difference between the collector of Q1 and the center point of the two resistors R1 and R2, which is amplified and fed back to the base of Q1.
- Q1's collector voltage holds quite accurately at half the supply voltage plus one  $V_{BE}$  because of the gain in the feedback loop.
- Gain changes with temperature in all of the transistors are corrected for, and no adjustable resistor is required.
- The bias circuit has to be carefully bypassed at both high and low frequencies.

## FET Bias

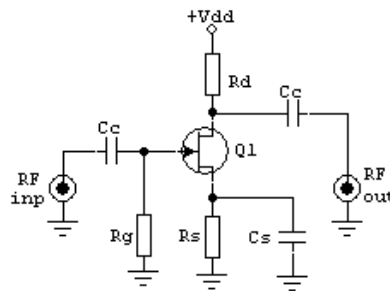
Bias networks are what are used to put a FET at the intended **quiescent operating point**. For example, you might want to operate a FET in a power amplifier at 12 volts VDS and at 50% of the saturated drain current ( $I_{DSS}/2$ ). This is the quiescent point.

The same as in BJT case there are at least three ways to bias up a FET amplifier to get to the intended quiescent operating point.

One option is to have separate DC power supplies for the gate and drain connections, with the gate supply being adjustable, and ground the source. Grounding the source will provide the most gain and efficiency from the FET. In this case generally the gate bias supply is a fixed negative power supply - 5 Volts, with an adjustable resistor-divider network being employed to supply the needed gate voltage.

Another method of biasing a FET is with an **active bias** network, generally designed in a feedback configuration to maintain constant quiescent current.

Common-source FET's can utilize a common Class-A biasing technique called **source bias**, a form of **self bias**.

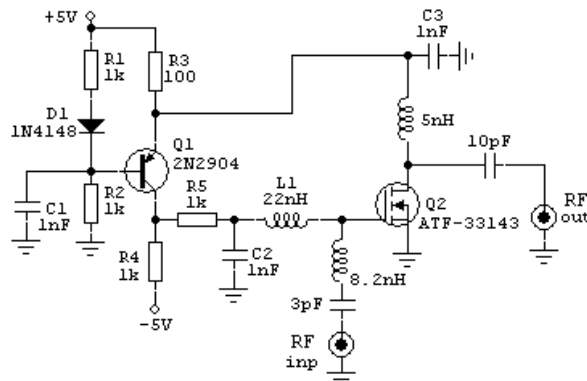


FET Source Bias

- With FET's, unlike BJT's, no gate current will flow with an input signal present, so the drain current will always be equal to the source current.
- However, source current does flow through the source resistor  $R_S$ , creating a positive voltage at the top of this resistor.
- Since the FET's source is shared by both the drain and the gate circuits, and the gate will always be at 0V with respect to ground (since no gate current equals no voltage drop across  $R_G$ ), then the gate is now negative with respect to the common source. This allows the FET to be biased at its Class A, AB, or B quiescent currents  $I_{cq}$ 's, depending on the value chosen for  $R_S$ , while a capacitor can be inserted across  $R_S$  in order to restrain the bias voltage to a steady DC value.
- The Source de-coupling capacitor  $C_S$  is required to ensure that there is no RF power loss on  $R_S$ .
- The downsides to using self-bias schemes are that amplifier efficiency is lost due to the voltage drop of the source resistor.

### FET Active Feedback bias example:

Suppose that we have the following GaAs FET bias circuit:



432MHz GaAs-FET LNA

1. The DC current through diode D1 increases (due to temperature variation or change in device)
2. Then, the voltage drop across R3 will increase, reducing  $V_{BE}$ , Q1.
3. The collector current of Q1 drops, reducing the voltage drop across R4. This reduces  $V_{GS}$  and  $I_D$  of Q2 to correct for the change in step 1.

## GaAs FET Bias

The most important characteristic to consider when designing a bias circuit for small signal GaAs FETs is the previously mentioned transfer characteristic.

Generally, two methods can be used to bias a GaAs FET:

### 1. Dual Power Source Method

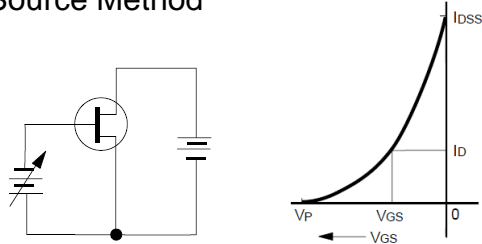


Figure above shows a GaAs FET bias circuit which uses the dual power source method. Since the condition  $V_P < V_{GS} < 0$  must always apply to a GaAs FET,  $V_{GS}$  can be derived from:

$$V_{GS} = V_P \left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right)$$

### 2. Self-Bias Method (Auto-Bias)

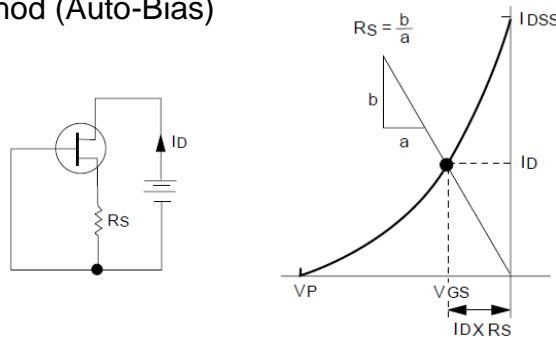


Figure above shows the most universal method for reducing electrical potential between the gate and the source when there is only one power source. If the source resistance is  $R_S$ , and the operating current is  $I_D$ , then the drop in electric potential caused by  $R_S$  will be:  $I_D * R_S$

The actual electrical potential between the gate and the source will be:  $V_{GS} = -I_D * R_S$

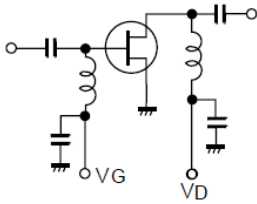
## GaAs FETs typical biasing methods for high frequencies:

Figures and tables below show the five general bias types for GaAs FETs: **a**, **b**, **c**, **d**, and **e**.

- Type **a** is the previously described dual power source bias method appropriate for use in the higher frequencies. When directly connecting the source to the ground terminal, source inductance can be made relatively small. By using this method, higher gain can be obtained and a lower noise factor anticipated in the higher frequencies.
- All other bias methods insert a bypass capacitor into the source. Even if the high frequency performance of the bypass capacitors can be guaranteed, there will always be a loss ( $\tan \delta$ ) resulting from the material's dielectric properties. Even with chip capacitors, there is always some inductance and care must be exercised when using them at higher frequencies.

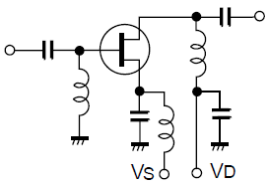
- Types **d** and **e** require only one power source. They are compatible with the previously described method. An advantage of this method is that if the source voltage should increase for any reason, that increase will be proportionate to the drop-in potential caused by  $R_s$ , which is connected in series with the source,  $R_s * \Delta I_D$
- $\Delta I_D$  is the increment in drain current caused by the increment in source voltage. Drain current increase will be automatically suppressed, due to the proportionate negative bias on the gate. Generally, if a single source type (self-biasing type) is selected, **d** is used; if the only available source is a negative one, then **e** should be selected.
- Tables below also shows the order for adding bias when a dual power source is used. This is to prevent, as much as possible, a large current from flowing through the GaAs FET.

a)



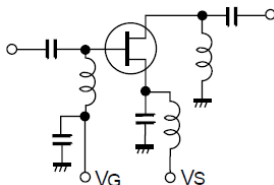
Bias Voltage	Bias Order	Bias Polarity
$V_G$	1	Negative
$V_D$	2	Positive

b)



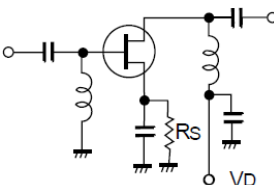
Bias Voltage	Bias Order	Bias Polarity
$V_S$	1	Positive
$V_D$	2	Positive

c)



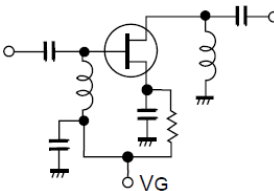
Bias Voltage	Bias Order	Bias Polarity
$V_G$	1	Negative
$V_S$	2	Negative

d)



Bias Voltage	Bias Polarity
$V_D$ Only	Positive

e)



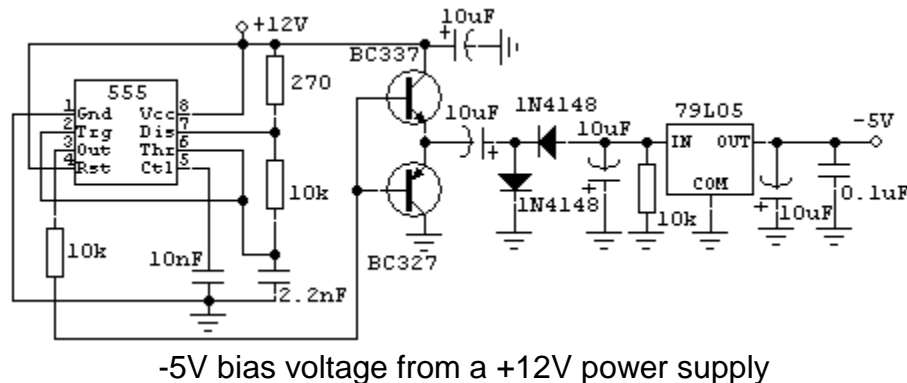
Bias Voltage	Bias Polarity
$V_G$ Only	Negative

#### Five general bias types for GaAs FETs

- The GaAs FET generally has a high mutual conductance, giving it excellent frequency characteristics.
- If the gate voltage is near zero,  $g_m$  is at a maximum and oscillation may occur. For this reason, a bias scheme should be adopted that first applies a negative bias to the gate and then turns on the drain with a positive bias.
- There are slight differences between a bias circuit for a small signal GaAs FET and one for a power GaAs FET, but the above methods can be considered for both.

## Example of a negative -5V supply voltage for biasing GaAs FET's

The following circuit is providing a -5V bias voltage from a positive +12V power supply. The inverter is based on a NE555 circuit followed by a push-pull amplifier and a voltage doubler detector. The oscillation frequency is approximately 32kHz, which must be well DC filtered at the output to don't pass through the bias of the RF circuits.



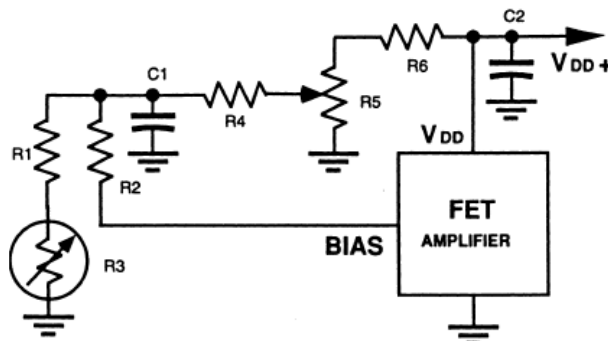
-5V bias voltage from a +12V power supply

## MOSFET Bias

Since MOSFETs have gate threshold voltages up to 5 to 6 volts, they require some gate bias voltage in most applications. They can be operated in Class C (zero gate bias), but at a cost of low power gain.

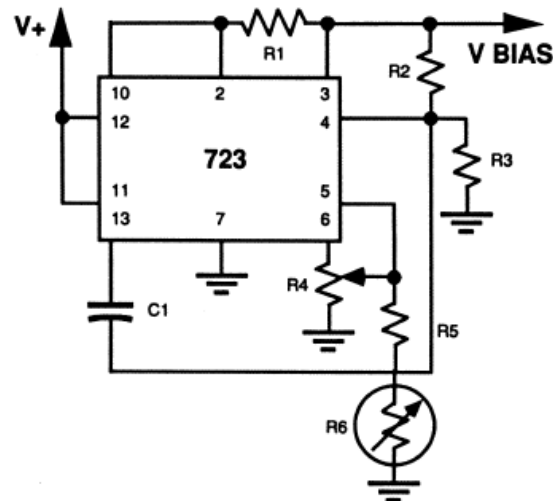
- Zero bias is often used in amplifiers intended for signals that do not need linear amplification (such as FM signals and some forms of CW signals), and efficiencies in excess of 80% are not uncommon.
- In Class B, the gate bias voltage is set just below the threshold, resulting in zero drain idle current flow. The power gain is higher than in Class C but the drain efficiency is 10 to 15% lower. Class B is also suitable only for non-linear amplification. Between classes of operation, one must decide whether the system has power gain to spare and how important efficiency is. At higher frequencies, such as UHF, a good compromise may be Class B or even Class AB.
- In Class AB, the gate bias voltage is somewhat higher than the device threshold, resulting in drain idle current flow. The idle current required to place the device in the linear mode of operation is usually given in a data sheet. In this respect, MOSFETs are much more sensitive to the level of idle current than are bipolar transistors. They also require somewhat higher current levels compared to bipolars of similar electrical size.

The temperature compensation of MOSFETs can be most readily accomplished with networks consisting of thermistors and resistors.



- The ratio of the two must be adjusted according to the thermistor characteristics and the  $g_{FS}$  of the FET. The changes in the gate threshold voltage are inversely proportional to temperature and amount to approximately 1 mV/°C. These changes have a larger effect on the  $I_{dq}$  of a FET with a high  $g_{FS}$  than one with a low  $g_{FS}$ . Unfortunately, the situation is complicated by the fact that  $g_{FS}$  is also reduced at elevated temperatures, making the drain idle current dependent on two variables.

The thermistor is thermally connected into a convenient location in the heat source in a manner similar to that described for the compensating diodes with bipolar units discussed earlier.



The circuit above shows a typical MOSFET bias voltage source using the 723 IC regulator. The temperature slope is adjusted by the ratio of the series resistor ( $R_5$ ) and the thermistor ( $R_6$ ). In addition to maintaining a constant bias voltage, this circuit also features a bias voltage regulation against changes in the power supply voltage.

#### MOSFET Closed-Loop Biasing

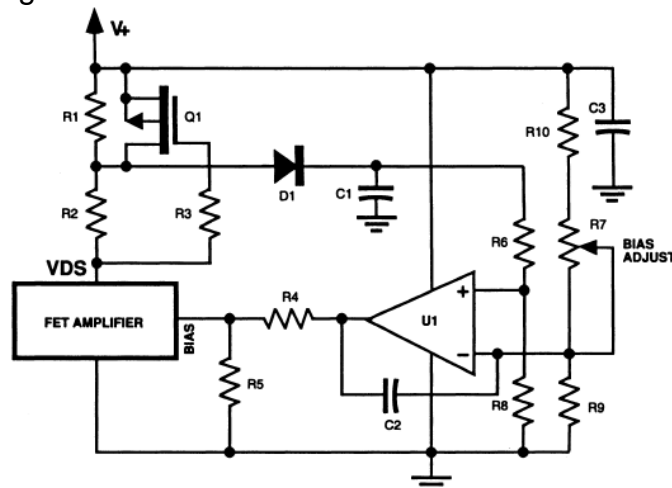
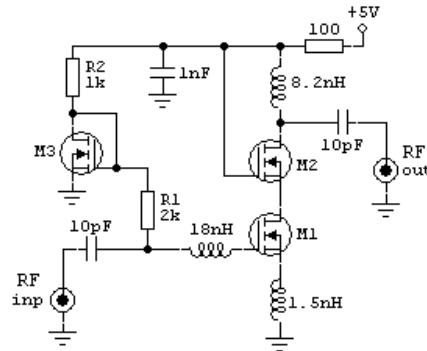


Figure above shows a Closed-Loop system for MOSFET biasing.

- It provides an automatic and precise temperature compensation to any MOSFET regardless of its electrical size and  $g_{FS}$ .
- No temperature sensing elements need be connected to the heat sink or to the device housing. In fact, FETs with different gate threshold voltages can be changed in the amplifier without affecting the level of the idle current. This means that the gate threshold voltage can vary within wide limits over short or long periods of time for a variety of reasons.
- In addition to temperature, other factors affecting  $V_{GS(th)}$  might be moisture, atmospheric pressure, etc.

The principle of operation of the circuit shown as follows: the idle current of the MOSFET amplifier is initially set to Class A, AB, or anywhere in between these bias limits by  $R_7$ , which also provides a stable voltage reference to the negative input of the operational amplifier  $U_1$ . Current flows through  $R_1$  with a consequent voltage generated across it. This voltage is fed to the positive input of  $U_1$ , which results in the output of  $U_1$  following it in polarity, but not in amplitude. Due to the voltage gain in  $U_1$ , which operates in D.C. open-loop mode, its output voltage excursions are much higher than those generated across  $R_1$ . Thus, if the current through  $R_1$  tends to increase for any reason, part of the output voltage of  $U_1$  fed to the amplifier gate bias input will adjust to

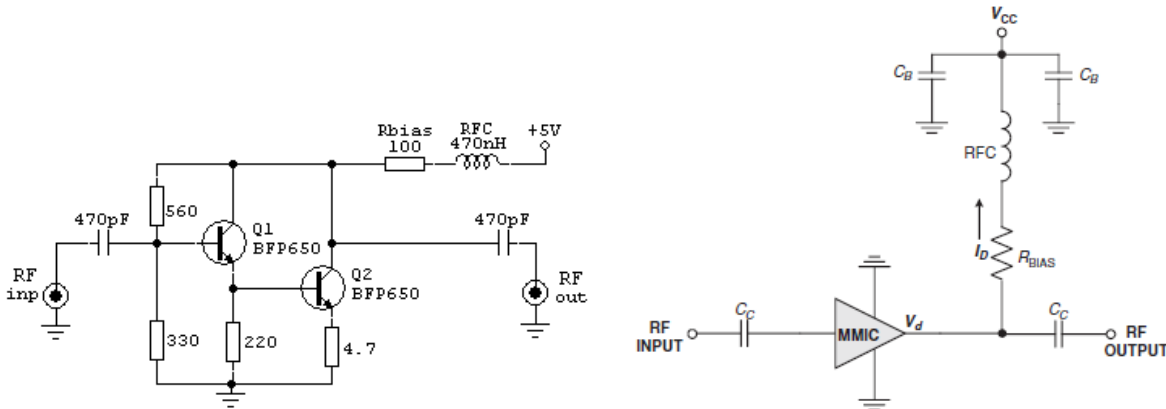
## Cascode MOSFET LNA Bias



Cascode MOS LNA

- Cascading transistor M2 is used to reduce interaction of the tuned output with tuned input.
- Transistor M3 essentially forms a current mirror with M1.
- The current through M3 is set by the supply voltage and R2 in conjunction with  $V_{GS}$  of M3. The bias resistor R1 is chosen large enough that its equivalent noise current is small enough to be ignored. In a 50 ohms system values of several hundred ohms to kilo ohms or so are adequate

## MMIC Amplifier Biasing



Typical MMIC internal schematic (DC blocking caps, Rbias and RFC are external components)

- The current-biased MMIC will attempt to draw more current as the temperature rises.
- The biasing is primarily determined by the current, where the voltage is relatively unimportant.
- The effectiveness of this temperature bias control is dependent on the voltage drop across  $R_{BIAS}$ , a value of up to 4 V may be required for proper stabilization across a minus 25°C to a plus 100°C temperature range.
- If the  $R_{BIAS}$  does not add up to 600Ω or more, then the gain of the MMIC stage will suffer.
- If  $R_{BIAS}$  does not compute to be at or over 600Ω, then an RFC should be added in series with  $R_{BIAS}$  to increase the output to this value, or approximately  $R_{BIAS} + XL > 600\Omega$ .
- These amplifiers are unconditionally stable at all frequencies, and they can be easily cascaded for higher gain.

The inductor bias-feed circuit is preferable to obtain low-noise performance, high gain, and linearity. By using an inductor as the bias feed, becomes constant and can increase in the large-signal region to extend its output power.

## Diode and Transistor bias for Linear Power Amplifiers

The use of Class-A and Class-AB amplifiers for linear power amplification relies on the use of a standing bias current, applied to the base (in case of BJT) in order to bias the RF device into partial or full conduction. This bias current must remain constant, despite the varying envelope of the input signal

When considering low power RF amplification, simple resistive biasing techniques may be used however, such techniques are not appropriate for medium or high-power amplifiers due to their requirement for low impedance, relative high current, voltage source.



- Whether employing diode or transistor bias, it is essential to thermally connect these components to the RF transistor itself. This allows the semiconductor bias components to track the power amplifier's temperature variations, and thus increase/ decrease the 0.7 V placed across Q1's base, maintaining the PA's collector current at a steady DC level. (As the temperatures rise, a silicon semiconductor junction's voltage decreases from its room temperature value of 0.7 V).
- Further, in order to force PA bias stability no matter what the input and output RF power levels may be, the standing current through the diode or transistor bias components must be high enough to permit a steady voltage to be maintained across the PA's base.



The clamping diode circuit presented above can be improved by the addition of an emitter follower to amplify the diode current, and hence reduce the required current through the diode by a factor to the current gain of the transistor used. The circuit employs two diodes in series, since one is required to compensate for the base emitter voltage drop of the transistor.



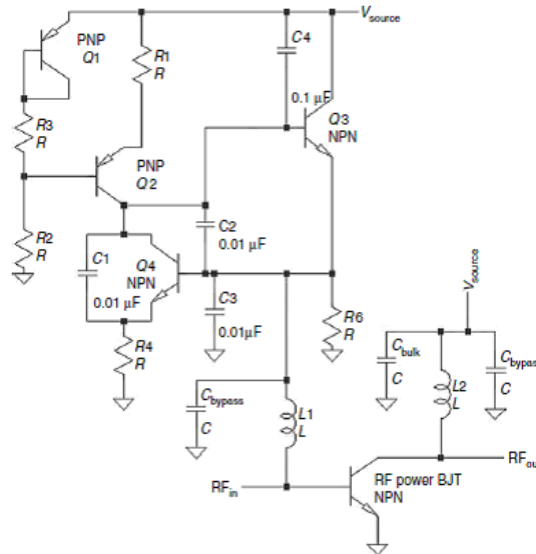
## Bias Modulation Effects

The function of a bias network is to supply an appropriate (and **constant**) voltage or current to the gate or base of the device. If the RF signals or their modulation are concerned, it should appear to be a high impedance at RF, and possibly a very low impedance in the case of modulation signals.

The bias design should not allow such signals to pass to any part of the power supply and the reflected back to the input of the active device. Signals at the modulation frequency (or harmonics) are generated by nonlinearities in the base or gate of the active device and these are often reflected, rather than absorbed by matching network. These modulation frequency signals must be absorbed by the bias network and not reflect back to the gate or the base of the device, otherwise there will be a modification of the IM products, and in the symmetry of the side shoulders.

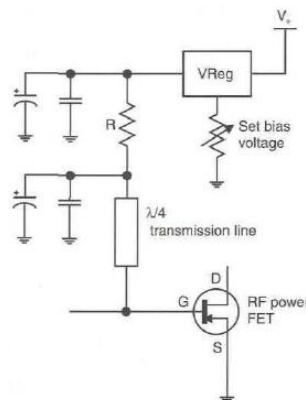
## Low Source-Impedance Active Biasing

Complex Thermal Compensated Bias circuit for Class-AB BJT Power Amplifiers



- This biasing scheme for RF power transistor provides near-constant low-frequency (1MHz) small-signal impedance presented at the base of RF transistor.
- The R2/R3 ratio it will set the bias current.
- This bias scheme is capable of providing independent control of bias impedance and class of the power amplifier for optimum efficiency and linearity.

## Power MOS-FET bias



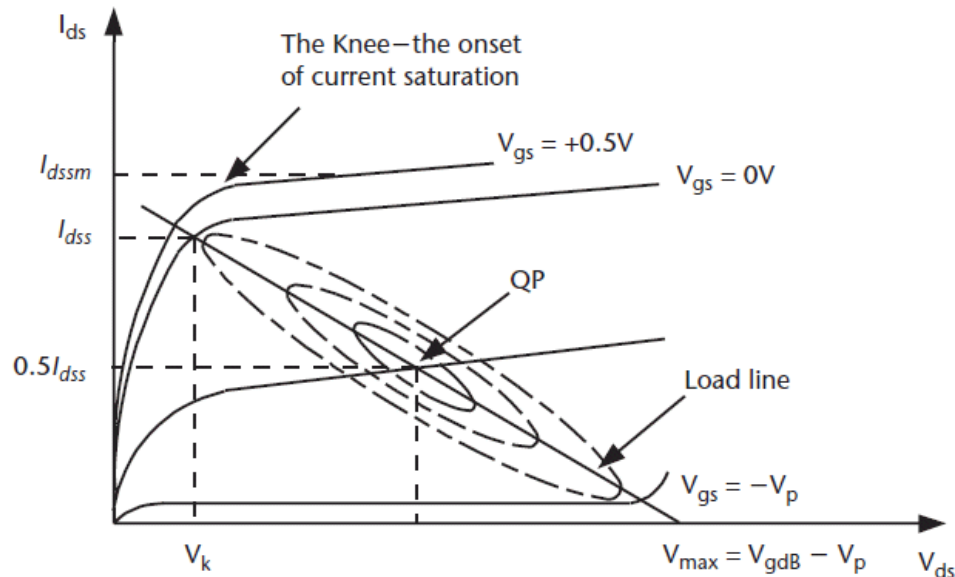
Biasing Power FET devices is usually simpler than biasing BJT devices. In many cases is sufficient to provide a bias voltage directly on the gate through suitable impedance. This impedance must be capable of minimizing the amount of RF feeding into the bias supply.

A typical network consists of a voltage supply (a variable voltage regulator) fed via a bias resistor whose primary function is to aid the decoupling of the gate from the bias supply, and a quarter-wave transmission line, which provides the RF isolation between gate and the bias supply.

## Power GaAs MESFET bias

Optimizing of the MESFET for maximum output power requires the device to be capable of sustaining large peak-voltage and current amplitudes.

A typical MESFET current vs voltage (I-V) illustrates that with positive gate bias, the MESFET can conduct current levels of 15% to 20% above saturated drain-source current  $I_{ds}$ .



Typically, Power MESFET Load line

- The maximum current is denoted as  $I_{dssm}$ , whereas  $I_{dss}$  is measured at zero gate-source bias.
- The transition from the linear operating region to the current saturation region occurs at the drain-to-source voltage above the knee voltage  $V_k$ .
- The highest voltage that can exist between the drain and the source is the gate-to-drain breakdown voltage  $V_{gdB}$  minus the pinch-off voltage  $V_p$ .
- This maximum voltage will be reached only as the drain current approaches zero.
- The drain-to-source voltages below  $V_k$  should be avoided because they imply high microwave losses in the non-saturation region.

The **Gate Biasing** of an RF power MESFET circuit has several functions:

- To maintain a constant  $V_{GS}$  gate-to-source voltage.
- To be able to supply a negative and positive  $I_{GS}$  gate current.
- To protect the gate by limiting  $I_{GS}$  when the device goes into breakdown (drain-to-gate or gate-to-source) or when the gate-to-source junction is biased with a positive voltage.
- These abnormal operating conditions for the devices can be due to an operator error, an overdrive, a system problem, or ESD (electrostatic discharge).
- To stabilize the device in case a negative resistance appears in the gate at any frequency where the device has a positive gain.
- To filter the signal, the products and the harmonics generated by the device input from low to high frequencies without affecting the device input matching circuit.
- To isolate the gate from any signal coming from the drain through the bias circuits.

The **Drain Bias** of an RF power MESFET circuit has several functions:

- To maintain a constant drain-to-source voltage.

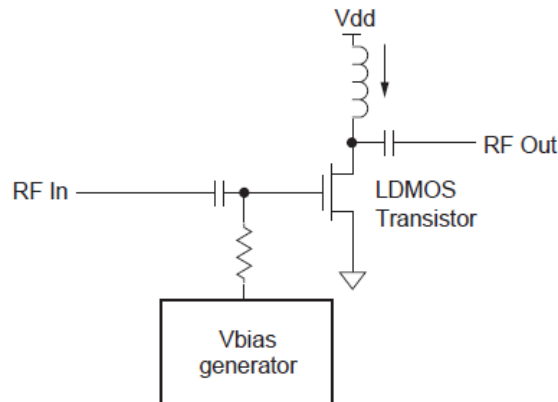
- To supply a drain current at least up to  $I_{DS}$  maximum under drive.
- To stabilize the device for the frequencies out of the amplifier bandwidth.
- To filter the signal, the products and harmonics generated by the device from low frequencies to high frequencies. It should be noted that as for the input biasing circuit the output biasing circuit also can be used as matching element.
- To isolate the gate from any signal from the output circuit.

## Power LDMOS Bias

LDMOS transistors are CMOS devices designed for high frequency, high voltage operation.

- LDMOS transistors exhibit an annoying characteristic called bias or  $I_{DQ}$  drift.
- All LDMOS parts exhibit the hot carrier injection effect to some degree.
- Hot carrier injection results in charge build-up in the gate-drain region, which causes the gate field to change. This is seen by the user as a change in the quiescent current ( $I_{DQ}$ ) with a fixed gate voltage.
- The use of adaptive bias circuits it requires a circuit that adjusts  $V_{GS}$  periodically to maintain a constant  $I_{DQ}$ .

A simplified circuit of an LDMOS amplifier bias circuit is shown below:



The DC bias on these amplifiers is set by applying a DC voltage to the gate ( $V_{GS}$ ) and monitoring the drain current ( $I_{DD}$ ). Ideally, this  $I_{DD}$  will be constant over temperature, but since the  $V_{GS}$  of LDMOS amplifier devices varies with temperature, some type of temperature compensation is required. One method of setting this DC bias involves using an adjustable reference, DAC, or Digital potentiometer combined with a temperature compensation source, such as a transistor  $V_{BE}$  multiplier.

A new way to bias an LDMOS amplifier involves digitally converting temperature information and adjusting the DC bias using Look-Up Table (LUT) memory. The memory is programmed at final test using measured parameters from the amplifier circuit being tested. DC bias performance is optimized over the required temperature range.

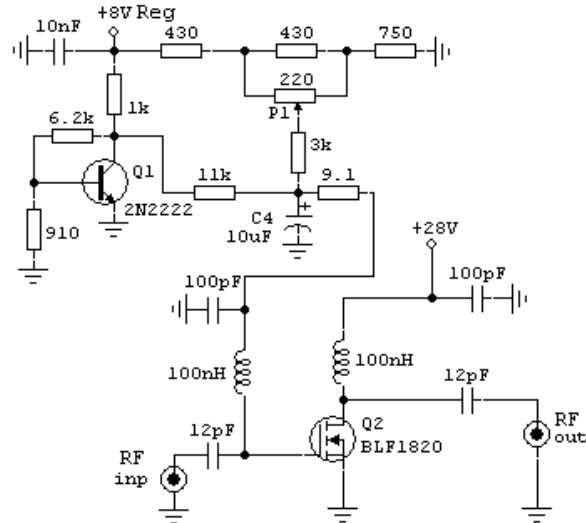
A very simple and effective way to construct the lookup table is to make measurements at two temperatures that represent the target range for the product, and then interpolate values for the other temperatures with a linear regression. A more accurate method would include more temperature points and then interpolate between those points.

LDMOS amplifiers also have a characteristic  $I_{DD}$  drift overtime (drain current reduces for a given  $V_{GS}$ ), as well as temperature. This can be addressed with lookup table correction with a slightly higher constant bias offset, so that over time the  $I_{DD}$  will drift closer to the target bias value, not further away.

LDMOS PA bias example:

The gate-source bias voltage is supplied through a voltage divider set by adjusting the potentiometer P1 to control the optimum Q2 drain current  $I_{dq}$ . In this example  $I_{dq}$  was set to 750 mA to

achieve the performances. Deviations from this optimal bias point will result in suboptimal trade-offs of performance parameters such as gain compression and efficiency. The device is more linear, but less efficient for the tune shown here at higher drain voltages. If the user has severe efficiency requirements, 26V may be more suitable on the drain. If the user has more requirements for linearity, 30V on the drain may be more appropriate.



LDMOS Power Amplifier with active bias and regulator

## Power GaN HEMT bias

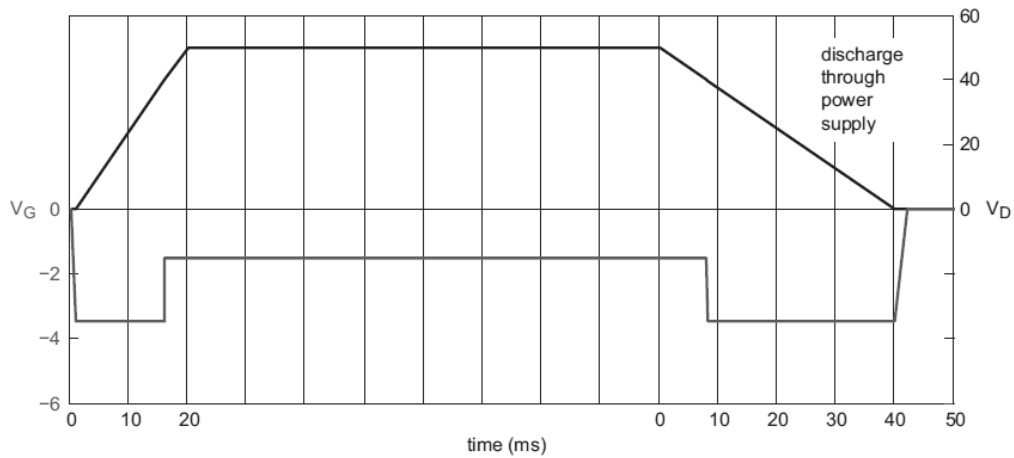
Power supply sequencing is critical while operating externally biased GaN power amplifiers:

- Failing to follow the proper power supply sequencing compromises the reliability of the device.
- Exceeding breakdown voltage levels can result in instant failure.
- Long term reliability degrades when out of bond conditions are repeated multiple times, and the system is stressed. In addition, continually violating the sequencing pattern damages the on-chip protection circuitry and results in long term damage, which can result in a failure in the field operation.
- Optimizing the bias level not only during power up and power down but also during regular operation can improve the performance of the RF amplifier, depending on the configuration and the application requirements. For example, the output power can be increased or decreased function of various system requirements. The external gate control of the power amplifier can implement these arrangements.
- Similar to LDMOS devices, GaN HEMT RF power transistors require temperature-compensated gate bias voltages, to maintain constant quiescent drain currents with temperature.
- GaN HEMT are depletion mode devices requiring **special bias and power sequencing** compared to LDMOS devices.

The most important consideration for DC bias with GaN HEMTs, is the **Bias Sequencing**.

Regarding GaN bias sequencing there are two issues to consider:

- Never apply drain voltage when the gate is at 0 V, as the device draws excessive drain current. Thus, any GaN bias controller must include sequenced drain voltage switching.
- For a given  $V_{GS}$ , GaN HEMTs are likely to be potentially unstable at lower  $V_{DS}$ . Therefore, decrease the gate voltage to below the pinch-off voltage  $V_P$  (such as -3 V) while the drain voltage is being turned ON and OFF.



Typical bias discharge time and levels of a GaN device ( $V_D$  upper line, and  $V_G$  lower line)

- It is important that  $V_{GS}$  is held at a voltage of less than  $V_P$  until  $V_{DS}$  is less than about +10V.

#### The **Gate Current** of GaN devices:

Because the GaN HEMT gate terminal is a Schottky diode, bias generators must provide significant amounts of both positive and negative gate current:

- GaN HEMTs have higher gate leakage currents than comparable LDMOS devices. The negative gate current evaluates to -5mA for a 100W device operating at 200°C junction temperature. When the device is driven into saturation, rectified positive gate current flows into the gate diode, and at heavy RF compression, the gate current could be about -30mA for a 100W device.

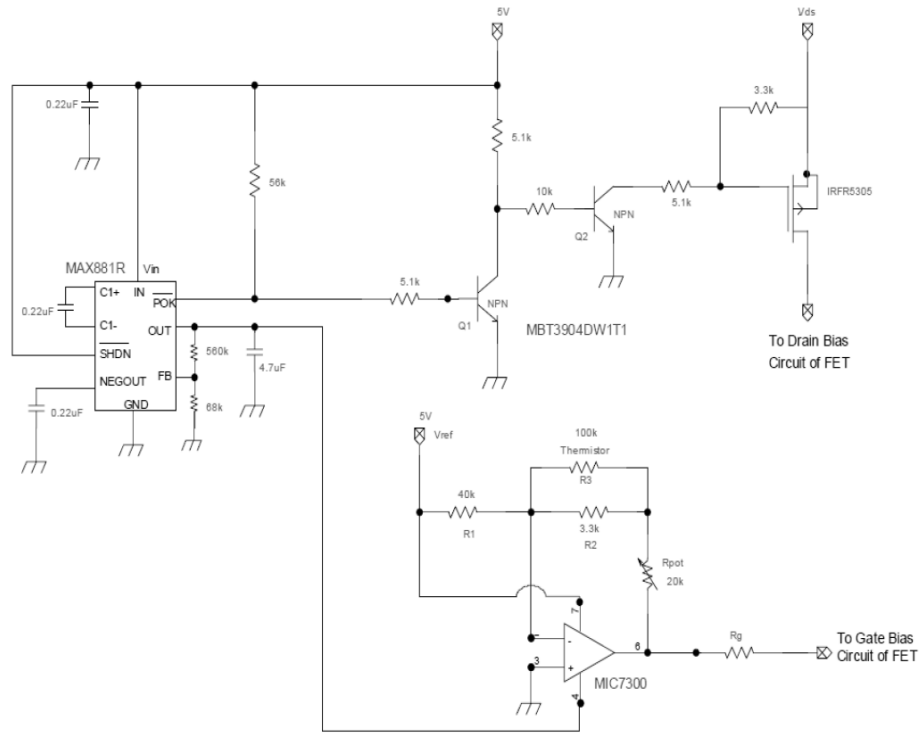
#### GaN **Bias Temperature Compensation**:

Similar to LDMOS RF devices, the gate threshold voltage for GaN RF devices is approximately proportional to temperature.

- The gate threshold voltage is the voltage required to maintain a constant quiescent drain current, which is generally about +1mV/°C junction temperature. However, practical temperature compensation circuits shall mandatory monitor the case temperature of the GaN device, where the temperature change is typically only half the junction temperature change. Thus, the bias controller must increase  $V_{GS}$  by about +2mV/°C.

#### GaN **sequence bias example**:

As is shown in the schematic below, most of lower power GaN HEMT bias controllers use a P-channel power MOSFET as the drain voltage load switch. This circuit has the advantage of simplicity, often requiring nothing more than level-shifting transistors between the voltage inverter “power valid” signal and the GaN MOSFET gate.



Circuit example for sequence biasing of a GaN HEMT device

The above bias sequence controller uses a MAX881 (charge-pump inverter) followed by a negative linear regulator, and a low-cost MIC7300 operational amplifier to drive the gate of the N-channel GaN device.

In addition to bias sequencing, the circuit also provides temperature compensation to the GaN RF power transistor by changing the gate voltage to assure constant drain current.

The thermistor R3 should ideally be placed as close as possible to the GaN power transistor to measure its temperature accurately.

This thermistor is placed in the feedback loop of the MIC7300 operational amplifier, such that the feedback tracks the gate voltage required to maintain constant drain current. In addition, the quiescent drain current at a reference temperature is set by Rpot. The exact temperature coefficient of the gate voltage is set by the values of R1 and R2 in unison with the thermistor.

However, as load currents increase above few Amps, the required P-MOSFET becomes large and expensive.

## Oscillators Bias Circuits

For the design a low phase-noise oscillator, the biasing circuit should be properly regulated and filtered to avoid any unwanted signal modulation or noise injection. Variations on the supply voltages or currents may also cause undesirable output power fluctuations and frequency drift.

Oscillator biasing of its amplifier section is employed for multiple reasons:

- To allow the use of a single  $V_{CC}$ ;
- to position the bias point for a certain class of operation
- to swamp out any device variations in beta
- to stabilize the active device over wide temperature variations.
- some oscillator topologies use noise feedback bias for phase noise cancellation.

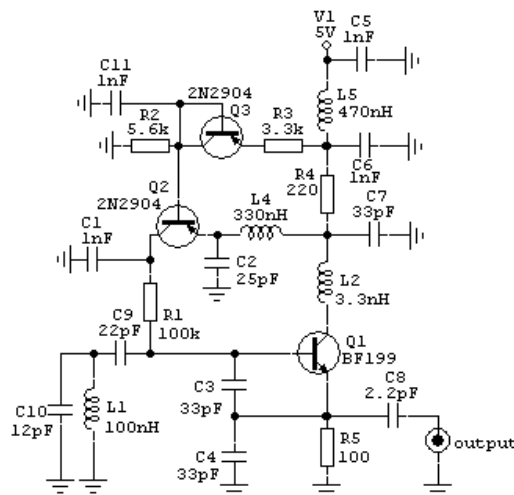
For accurate design of the bias of the oscillator, to meet the gain and phase conditions ( $G \geq 0\text{dB}$ , Phase shift around the loop =  $0^\circ$ ) the closed-loop feedback can be broken in an open-loop analysis. The circuit can be further tuned for optimal performance, in terms of gain and phase margin.

Few bias conditions shall be followed for best oscillator design:

- Minimize the oscillator's transistor bias current as much as possible, since this can substantially lower the  $1/f$  (flicker) noise frequency of the active device, as well as optimize the BJT's noise figure.
- Avoid driving the oscillator's transistor too far into compression. Most oscillators are biased for equivalent Class-A operation.
- For near-class-A operation oscillator, if limiting is due to cutoff, the oscillation amplitude is proportional to the emitter bias current.
- If limiting is due to saturation, the amplitude is proportional to the quiescent dc collector-emitter voltage. These parameters may be established with nearly any desired degree of stability by the selection of bias network type and complexity.
- In a well-designed near-class-A oscillator, the frequency is determined primarily by the resonator. As the loaded Q is increased, the active-device reactances become less significant in determining the oscillation frequency. Changes in these parameters from device to device, with temperature and with supply voltage, have less effect.
- A simple test of how well the active-device reactances are isolated from the resonator is to observe the operating frequency as the supply voltage is varied.
- The simplest method of ensuring near-class-A operation is to design the resonator amplifier cascade with small excess loop gain. The problem with this approach is ensuring that the loop gain does not fall below unity with temperature, device, loading, or other circuit changes. A second problem is that starting in an oscillator with low loop gain is slower.

### Oscillator with Noise Feedback cancellation

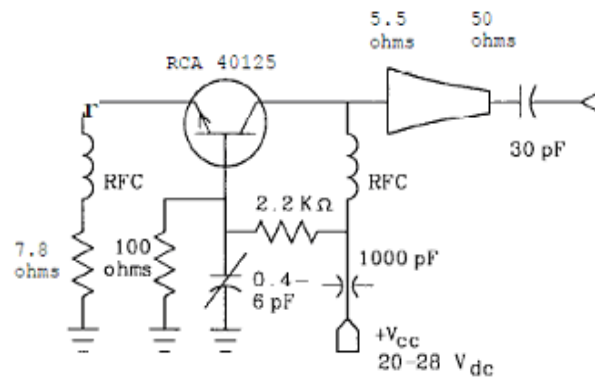
- The DC control PNP transistor Q2 acts both as a DC bias stabilization transistor and a noise feedback.
- This type of feedback bias circuit can provide a drastic noise improvement within the loop bandwidth of the circuit used.
- The noise sampling is done in the collector of Q1.
- Q3 connected as a diode provide temperature stabilization.
- The noise improvement can be expanded to 1 MHz off the carrier if the feedback circuit has the appropriate gain and exactly  $180^\circ$  phase shift within the required bandwidth.



150MHz Oscillator with Noise cancellation feedback bias

## Class-C Power Oscillators:

When high output power is required, and stability and noise are of less concern, the oscillator may be biased for class-C operation.



High Power Class-C L-band Oscillator

This oscillator has an output power of 2 watts with an efficiency of nearly 30%.

The bias is very “stiff.” There is no collector resistor and the emitter resistance is only 7.8 ohms.

High peak currents, limited primarily by the transistor, flow for a small fraction of the waveform period, but supply substantial power to the tank.

## RF Bias Circuit Issues

- Any emitter bias resistor and emitter capacitor can create low-frequency instability and bias oscillations, as well as increasing the NF and decreasing the gain of an amplifier. This demands that RF transistors have a directly grounded emitter lead, with no emitter feedback caused by the lead wire inductance.
- Thermal compensation is a concern for most bias circuitries because the bias point for a particular quiescent current will change with temperature. All devices experience this phenomenon, and in some cases (Bipolar transistors) the current gain will change with a positive coefficient eventually causing device destruction if the thermal effects are not accommodated in a bias circuit.
- While a BJT will change at fixed rate of  $-2.4 \text{ mV}/^\circ\text{C}$ , a FET has an inconsistent bias point rate of change with temperature and therefore will have to be empirically measured over the expected operating temperature range for the device chosen.
- Supply Modulation Effects - The variation in the current drawn from the power supply for a linear RF power amplifier ranges from almost zero for Class-A amplifiers, to the full current capability of the supply, for Class-B amplifiers. These large current variations should be isolated from the power supply circuitry (which usually has a poor RF and envelope frequency response) by means of the decoupling network. This filter network should be mounted as close as possible to the required point to ensure that all envelope frequencies are adequately decoupled.



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