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# **Service Manual**

For

**I 48 GTL**

**I 48 GTL ST**

**I 48 NW ST**

I 48 GTL  
I 48 GTL ST  
I 48 NW ST SM

# **Model 148 GTL / 148 GTL ST / 148 NW ST**

## **Table of Contents**

**Theory of Operations**

**Alignment Procedures**

**Exploded View / Parts List**

**Voltages**

**Schematics**

**Block Diagram**

**Bill of Material**

# THEORY OF OPERATION

## DETAILED DESCRIPTION

### 1. CIRCUIT FOR FREQUENCY STABILIZING

#### 1) Stability of Local Frequency

The local frequency is given by the following formula:

$$F_L = N \times F_r + 3 \times F_o$$

Fr : 10 KHz (Reference Frequency)  
Fo : off-set frequency

In the above formula, 10 KHz of Fr is given by dividing 10.24 MHz (XI) by 10224. As the N is limited by 123 on upper side, the total drift of N X Fr Accordingly, the frequency stability of the above FL is determined by stability of 3 X Fo.

The frequency tolerance of crystals used in the Fo (oof-set frequency) is kept within  $\pm 15$  PPM over the temperature range of  $-30^\circ\text{C}$  to  $+60^\circ\text{C}$ .

Each component value which may cause serious effect on the frequency is determined in minimize the effect of temperature change on the frequency tolerance of oscillator circuit is kept within  $\pm 20$  PPM.

Also, the supply voltage to variable capacitance diode (D35, D69) and oscillation circuit are supplied through the voltage regulator IC6 which minimizes the effect on the frequencies due to the change of supply voltage.

#### 2) Stability of Carrier Frequency

Another frequency which may cause the effect to the transmit frequency is the carrier frequency of 7.8 MHz band oscillated by TR32. The frequency tolerance of the crystal X4 is kept within  $\pm 20$  PPM over the temperature range of  $-30^\circ\text{C}$  to  $+60^\circ\text{C}$ .

Each component value which may cause serious effect on the frequency was determined to minimize the effect of temperature change on the frequency, and frequency tolerance of oscillator circuit is kept within  $\pm 25$  PPM.

Also, the voltage supply of oscillation circuit incorporates the voltage regulator IC6 which minimizes the effect on the frequencies due to the change of supply voltage.

## 2. CIRCUIT FOR DETERMINING FREQUENCY

### 1) Frequency Of The Transmitter Output

Transmitting frequency Ft, is produced in the Transmitter Mixer IC5 by mixing the local frequency FL is generated by the P.L.L. Local Oscillator circuit and is applied to one of inputs of IC5, and Fc generated by the Carrier Oscillator is applied to another input of IC5 after modulated and filtered in the case Frequency Ft as follows:

$$F_t = F_L - F_c$$

FL is determined in the P.L.L. Local Oscillator circuit dependent on the channel and the mode desired and Fc depends on the mode desired as shown in Table (Page 15).

## 2) P.L.L Local Oscillator Circuit

FL or the frequency of the voltage controlled oscillator (V.C.O.) is controlled by the phase locked loop (P.L.L.) synthesizer system as follows. The output frequency of the V.C.O (IC2) is applied to one of inputs of the In-loop Mixer TR20 and mixed with the off-set frequency which is generated by the off-set oscillator TR30 and the multiplied by three times by the tripler TR29. The resultant frequency of the difference between above frequency is produced on the output of TR20 as follows:

$$F_1 = FL - 3 \times F_o$$

F1 = Output frequency of TR20

Fo = off-set frequency, approximately, 11.325 on AM mode, 11.3255 MHz on USB mode and 11.3245 MHz on LSB mode.

3 X Fo : 33.975 MHz on AM mode, 33.9765 MHz on USB mode and 33.9735 MHz on LSB mode.

F1 falls into the range of 790 KHz to 1230 KHz at increment of 10 KHz.

F1 is applied to the PLL. IC, IC1, and is divided by programmed divide ratio "N", by divider. IC1 has an 8-bit binary programmable divider.

The resultant frequency is applied to the phase detector in IC1 and is compared or phase-detected with the reference frequency of 10 KHz applied to another input of the phase detector. The phase detector generates the control voltages for V.C.O. to minimize the difference between F1 divided by N and the reference frequency. Thus, under locked condition of the loop, the local frequency FL is locked stable and is calculated by the following formula:

$$FL = N \times 10 \text{ KHz} + 3 \times F_o$$

## 3) Channel Selection Program

The divide ratio, N, of the programmable frequency divider is determined by supplied voltage to the program input terminals, pin No. 11 through Pin No. 16 of the CI1.

The program data are programmed by the channel selector switch, S401 and are applied to CI1.

The function of the program input terminals is as follows:

Pin No. CH No.	11	12	13	14	15	16	Programmed Divide Ratio "N"
1	0	0	1	1	1	1	79
2	0	1	0	0	0	0	80
3	0	1	0	0	0	1	81
4	0	1	0	0	1	1	83
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
40	1	1	1	0	1	1	123
Remarks : "0" = Ov                      "1" = VDD							

#### 4) Transmitting Frequency Calculation

For an example, when the unit is operated on channel No. 19, the transmitting frequency is calculated as shown in the following table for each mode.

	AM mode	LSB mode	USB mode
N	101	101	101
3 X Fo (MHz)	33.975	33.9735	33.9765
N X 10 KHz(MHz)	1.01	1.01	1.01
FL (MHz)	34.985	34.9835	34.9865
Fc (MHz)	7.8000	7.7985	7.8015
Ft (MHz)	27.185	27.185	27.185

#### 5) Clarifier Circuit

In the receive operation, the control voltage varied by the clarifier control VR-402 is phased through the clarifier gate diode D51 and is applied to a variable capacitance diode which is connected to the off-set frequency oscillator Crystals.

The above mentioned circuit may vary the off-set frequency by means of rotating the clarifier control VR42 at the range of approximately  $\pm 1$  KHz.

In the transmit operation, clarifier gate diode D51 is reverse biased and that separates the variable capacitance diode from the clarifier control.

#### 6) Frequency Counter Circuit

A local frequency FL and a carrier frequency Fc are counted at IC506 in turns at an interval of 0.5 sec.

Then, the subtraction FL - Fc is performed by using IC502 and this result is displayed digitally.

### 3. FREQUENCY SYNTHESIZER

The synthesizer is consisted with the following components;

PLL IC (IC 1)

X-TAL (X 2)

Varicap Diode (D1)

IC 1 is a cmos LSI that includes most of PLL block. The VCO with varicap diode D1 as a part of the oscillator tank circuit.

### 4. Reference Frequency

The crystal, X 2(10.240 MHz) and other components at Pin 7,8 and of IC1 can make a reference frequency oscillator with internal amplifier.

### 5. VCO

TR1 is connected as a clamp type oscillator with varicap diode as part of the circuit.

With appropriate control voltage on also drives, the VCO can be oscillate over the required range of 34.765 MHz to 35.205 MHz.

### 6. Receiver Local Oscillator Outputs

#### **Fist Mixer:**

The secondary output of VCO tank circuit L20 is injected through buffer AMP TR2 to the base of 1'st mixer TR15.

#### **Second Mixer:**

The oscillation output, oscillated with 7.345 MHz signal is injected into the gate of FET4.

## 7. DESCRIPTION OF CIRCUITS

### 1) Transmitter

#### A. Circuit For Suppression Of Spurious Radiation

The tuning circuit between frequency synthesizer and TX final AMP TR36 and L35, L37, L38, L39, C149, C150 in the TR36 output circuit serve to suppress spurious radiation and SWR circuit to serve for impedance match TR36 to the antenna and to reduce spurious content to acceptable levels in the frequency synthesizer.

#### B. Circuit For Limiting Power

During the factory alignment the VR8, VR9, VR10. That the D49, D50, TR37 to compensator the temperature and bias controlling the TX final AMP (TR36) and TX driver (TR38) these component is selected to limit the available power to slightly more than 4 watts. The tuning is adjusted so that the actual power is from 3.6 to 4.4 watts for SSB circuit alignment VR11 for limiting power which this deepen on the input MIC signal that less or more.

#### C. Modulation

Modulation circuit produced each modulation signal of AM/SSB and supplies the signal to the transmitter mixer(IC5).

**AM mode:** The microphone feeds voice through TR23 and through TR22 and the switching TR21 to the power AF AMP IC6 and through the AM power REG. (TR41, TR42). Then is fed through the collector of driver TX. TR38 and the final TX. TR36 to collector modulation both these stages.

**SSB Mode:** The microphone feeds voice audio signal through TR23 and through TR22 and to the IC3 (Blanced modulator) IC3 mixes 7.8015 MHz for USB and 7.79850 MHZ for LSB with voice audio signal then produce DSB wave remove 7.8015 MHz or 7.79850 MHz (Deepen on USB/LSB) carrier signal through X-tal filter and only the signal wanted band is applied to IC5 TX mixer.

#### D. Circuit For Limiting Modulation

A portion of the modulation voltage is refitted by TR24 which attenuated the input signal from microphone, from the AM power REG. (TR41, TR42) the signal is feed back to the TR26 (AMC Controller) and through TR34 loop keeps the modulation will not exceed 100 percentage for input approximately 40 dB. the AF-ALC is adjusted by VR501.

## 2. RECEIVER

The receiver is a double conversation supper heterodyne

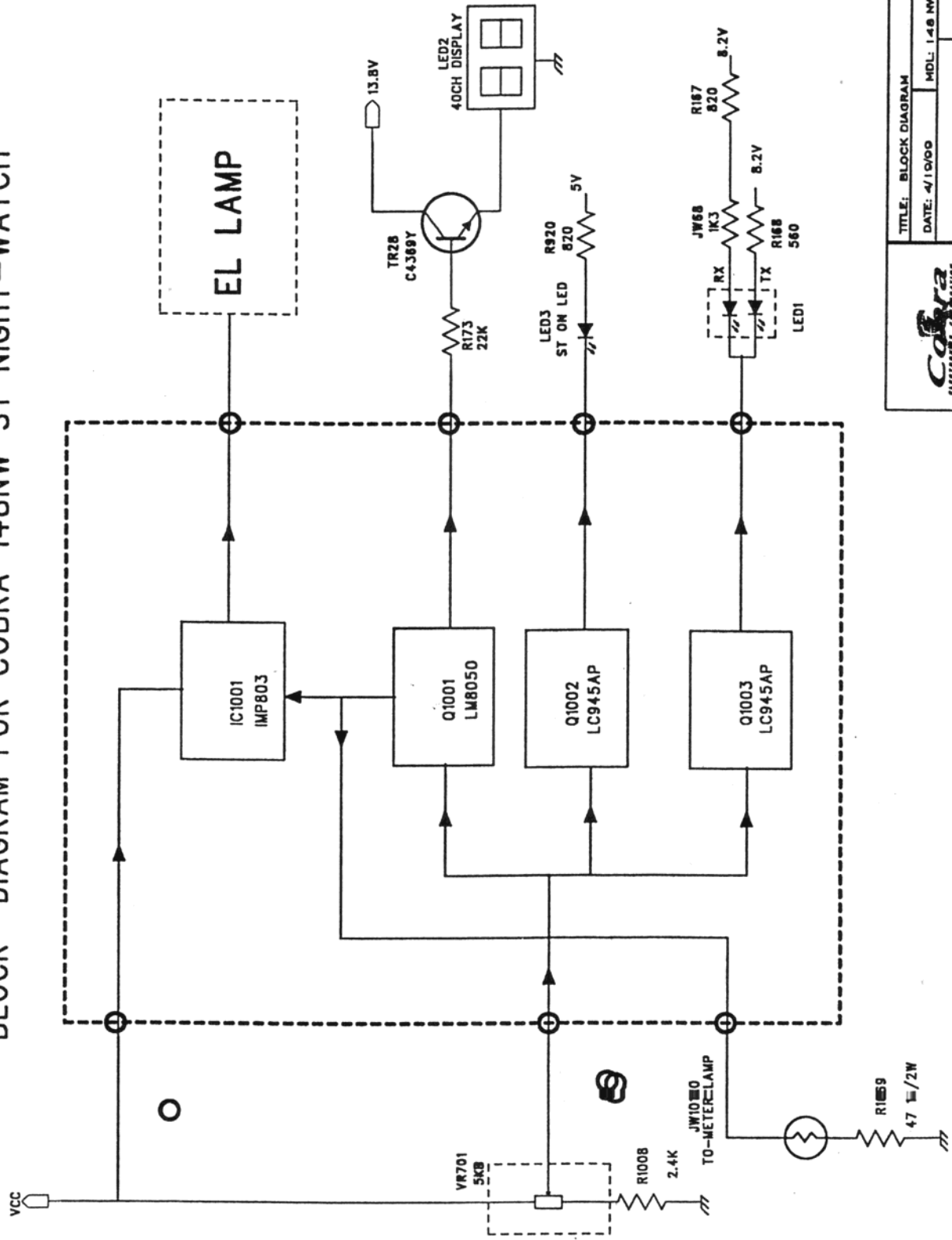
**AM Mode:** The first IF frequency at 7.8 MHz and the second IF frequency at 455 KHz. But the second local oscillator frequency is 7.345 MHz.

**SSB Mode:** The first IF frequency is 7.8 MHz these following by item #5.

All both systems squelch is controled by TR12 and TR13.



# BLOCK DIAGRAM FOR COBRA 148NW ST NIGHT-WATCH



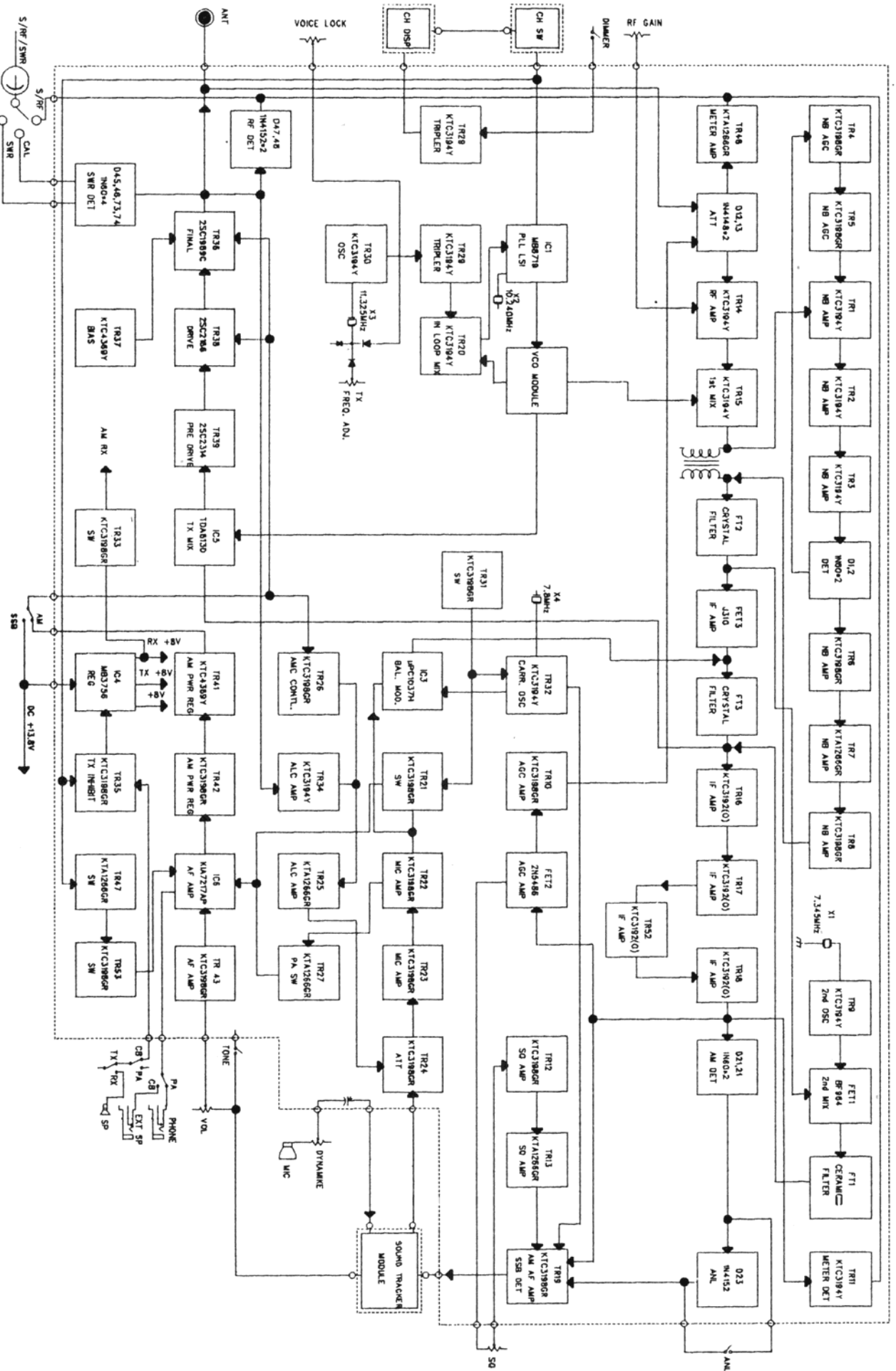
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ELECTRONICS

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CHICAGO, ILLINOIS 60707

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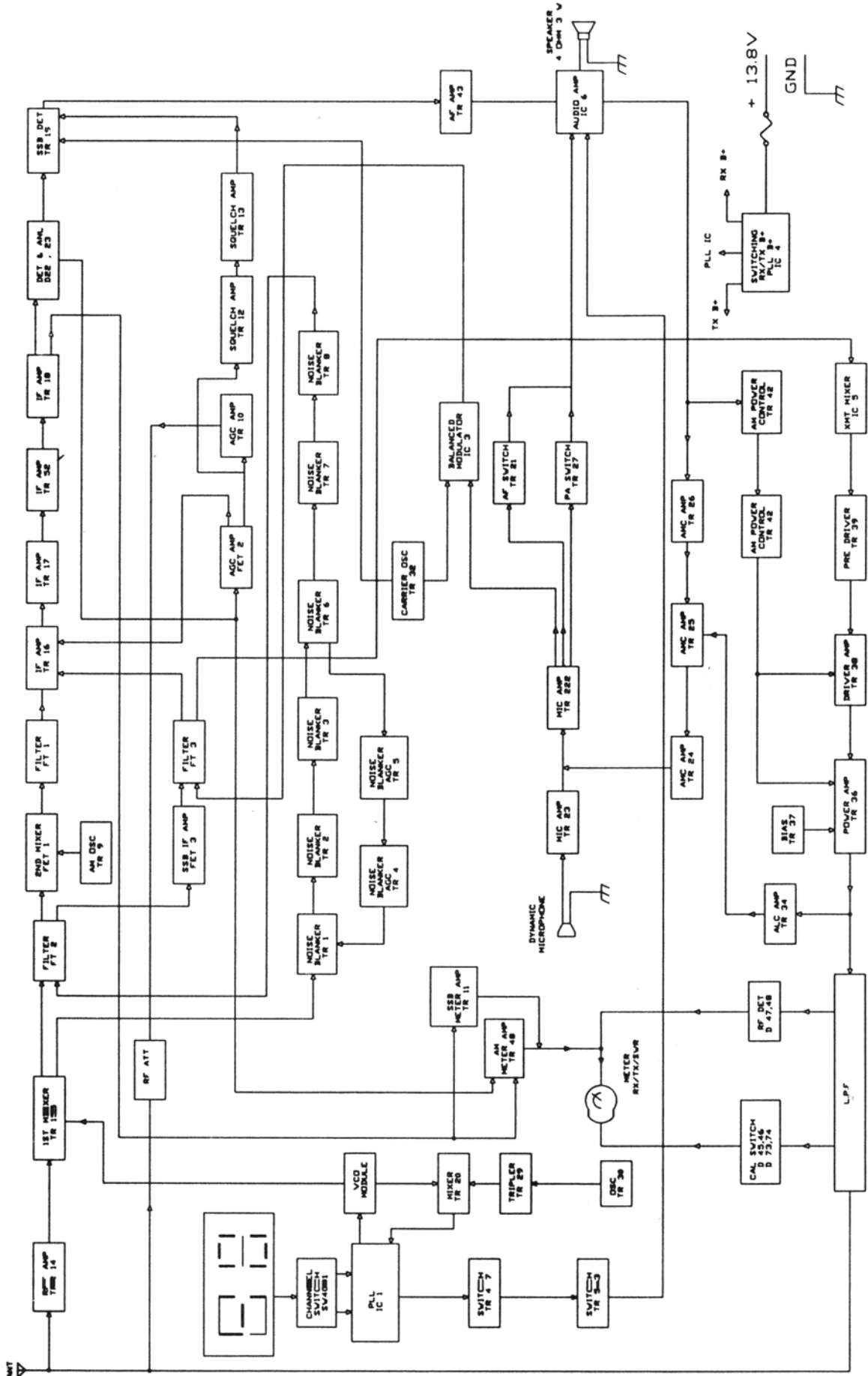
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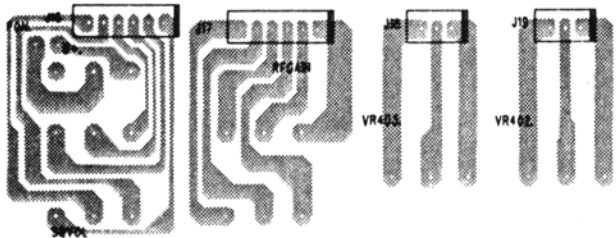
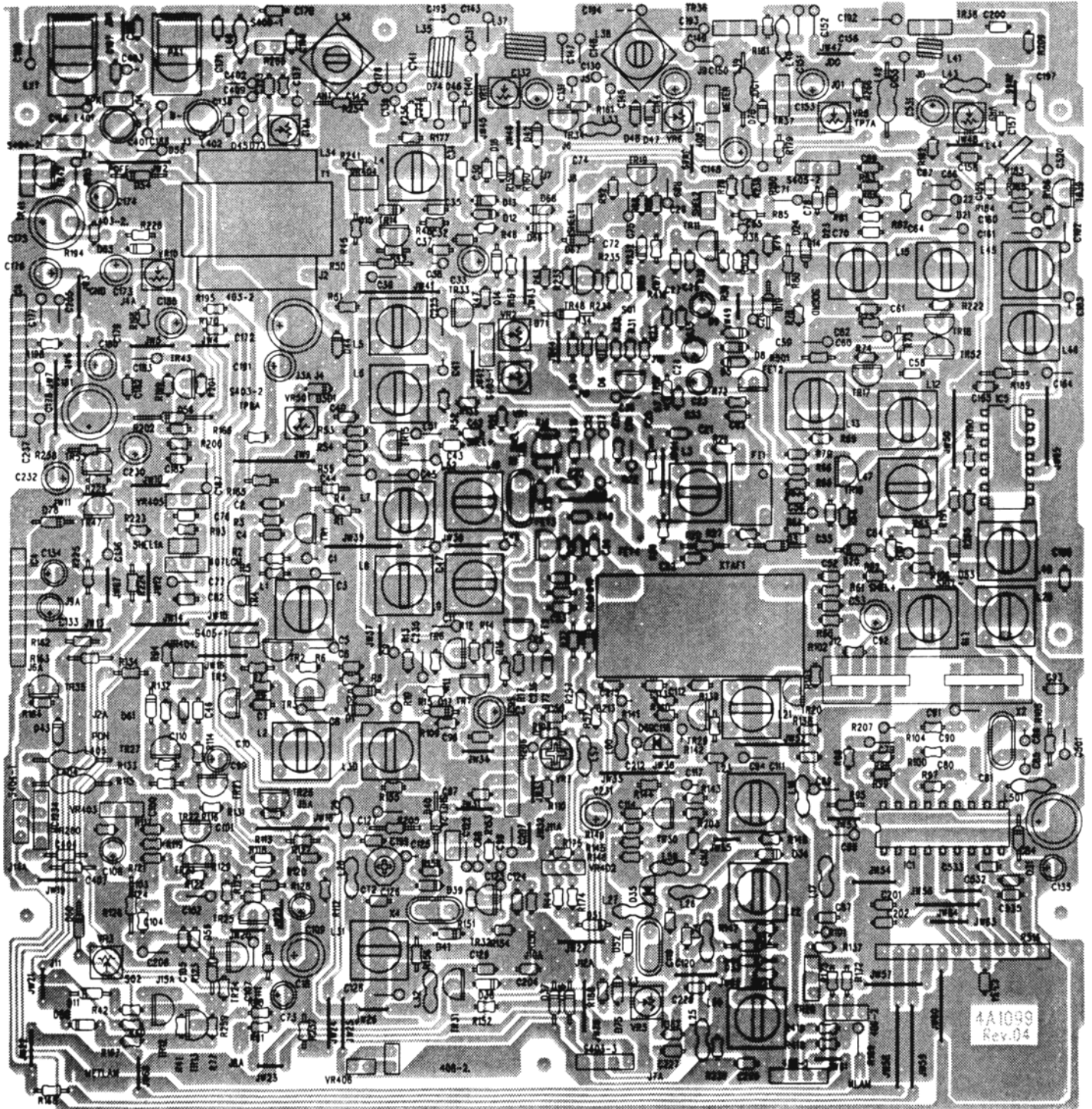


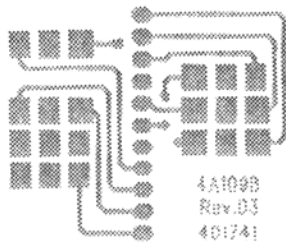
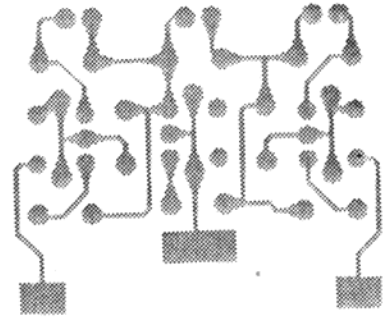
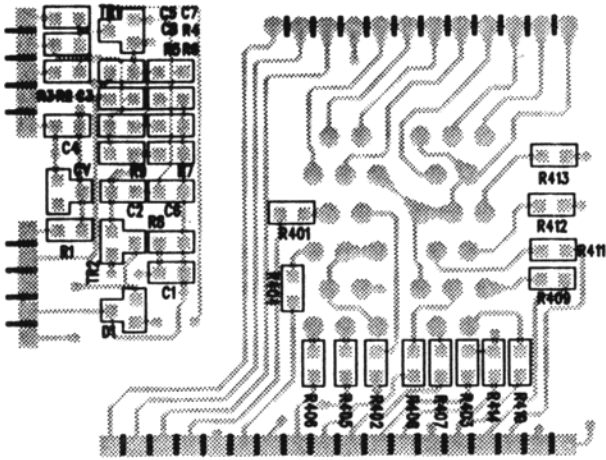
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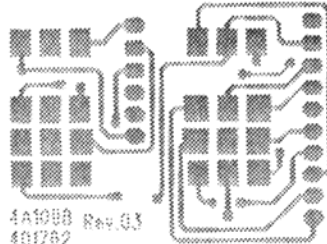


# TOP VIEW OF PCB BOARD

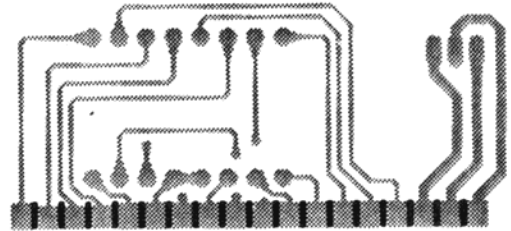




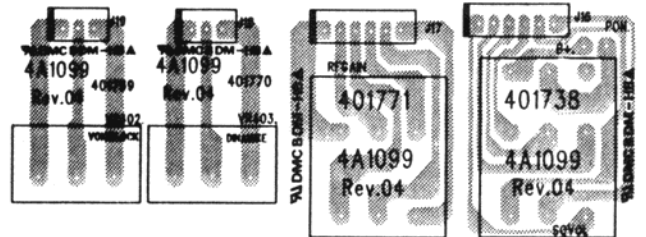
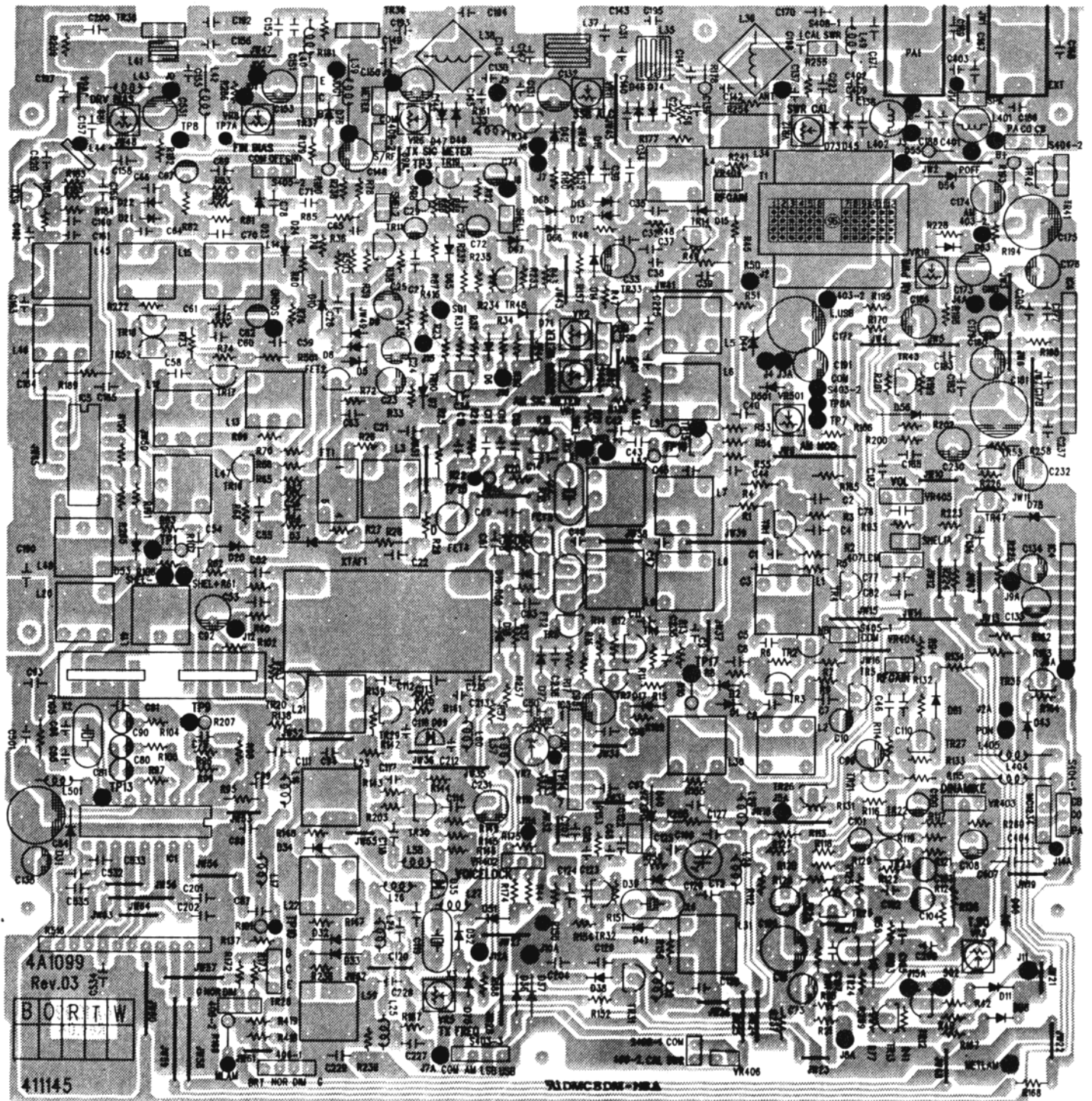
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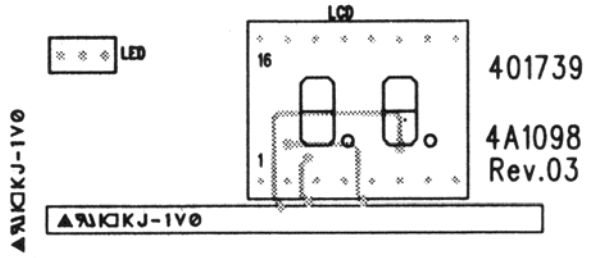
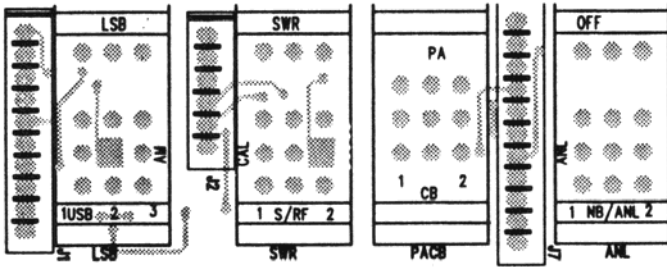
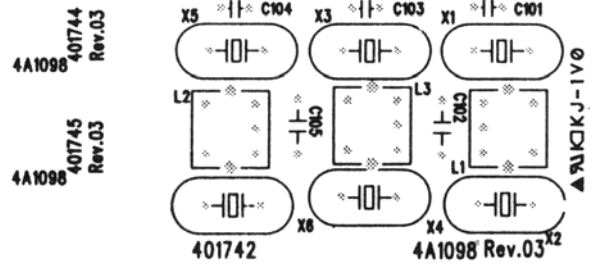
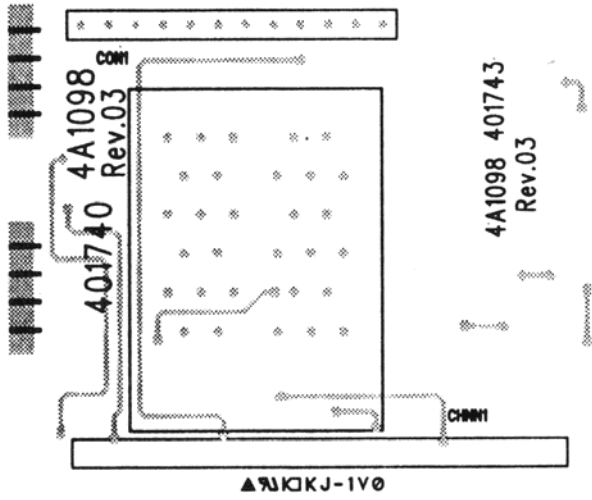


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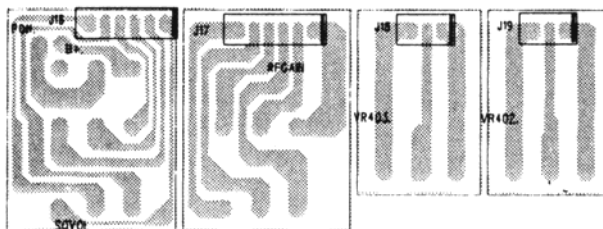
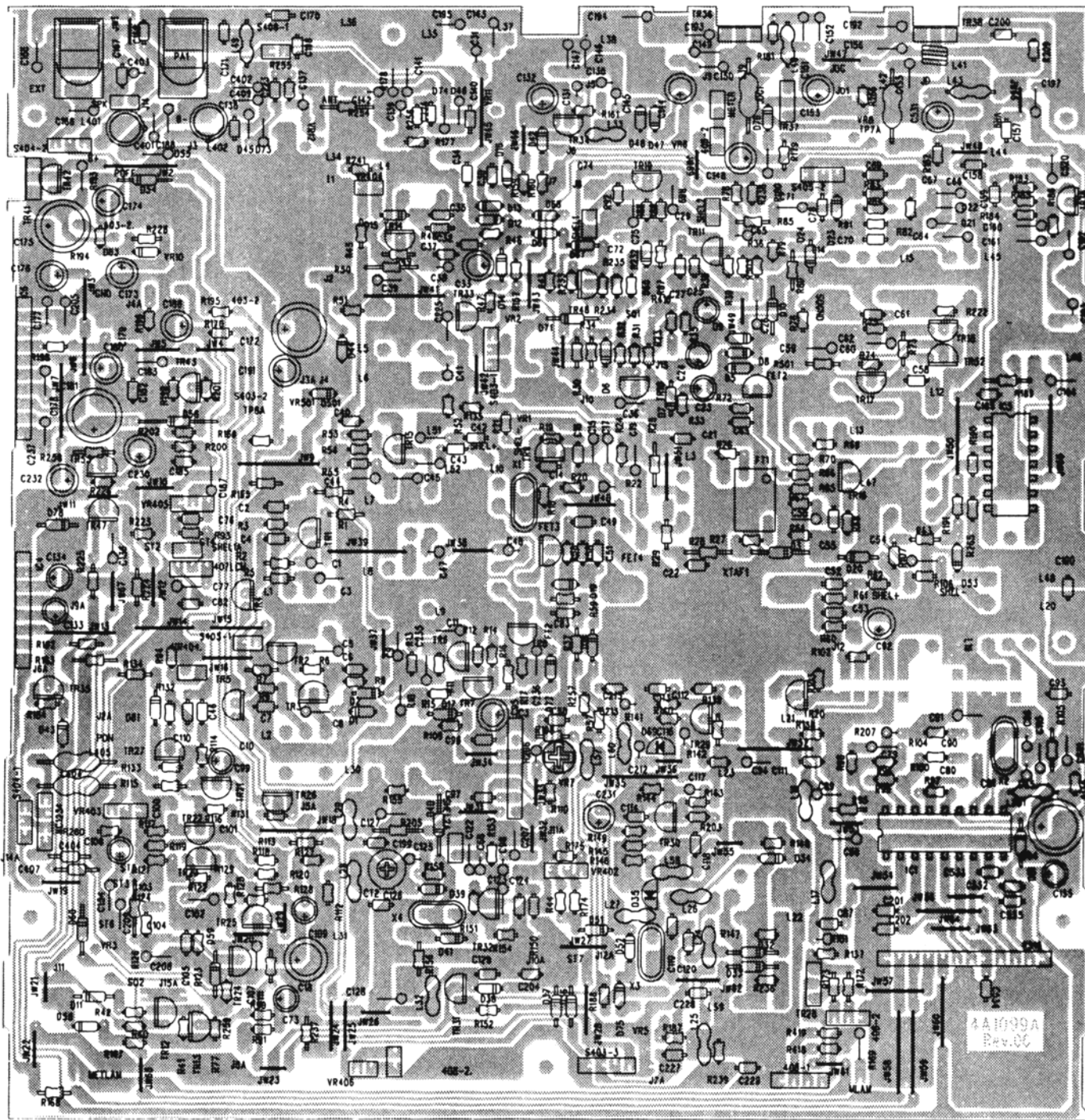
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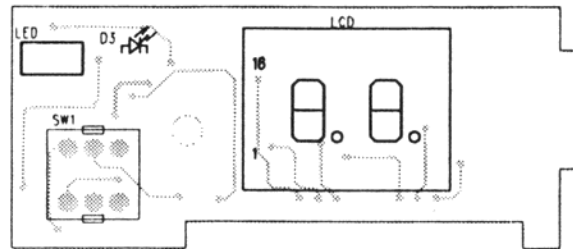
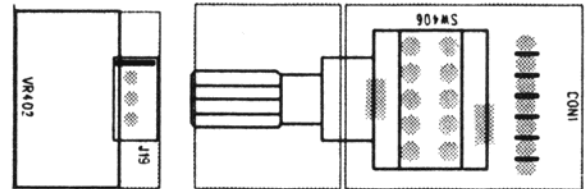
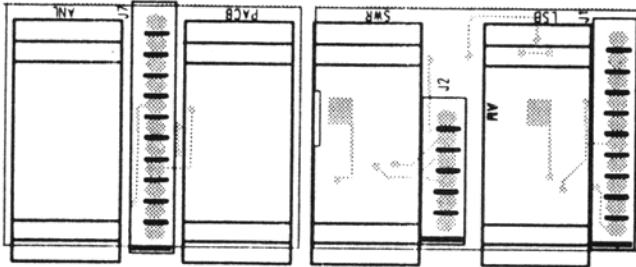
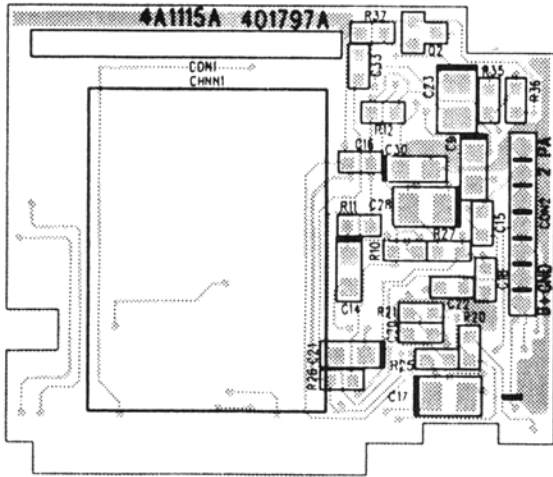


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# TOP VIEW OF PCB BOARD







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