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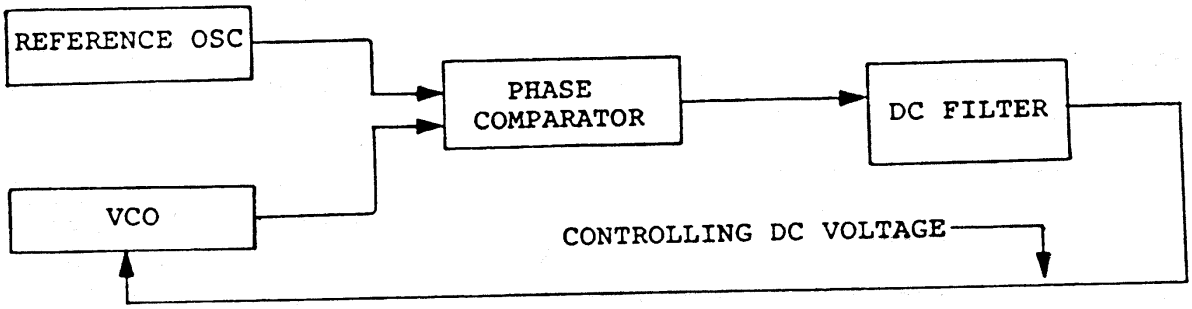
Model 20 Plus

OPERATING THEORY OF PLL FREQUENCY SYNTHESIZER
FOR MODEL 20 PLUS

1. Fundamental Theory Of PLL Circuitry

The purpose of PLL (Phase Locked Loop) circuit is to generate multiple number programable frequencies from a signal reference frequency with quartz crystal accuracy.

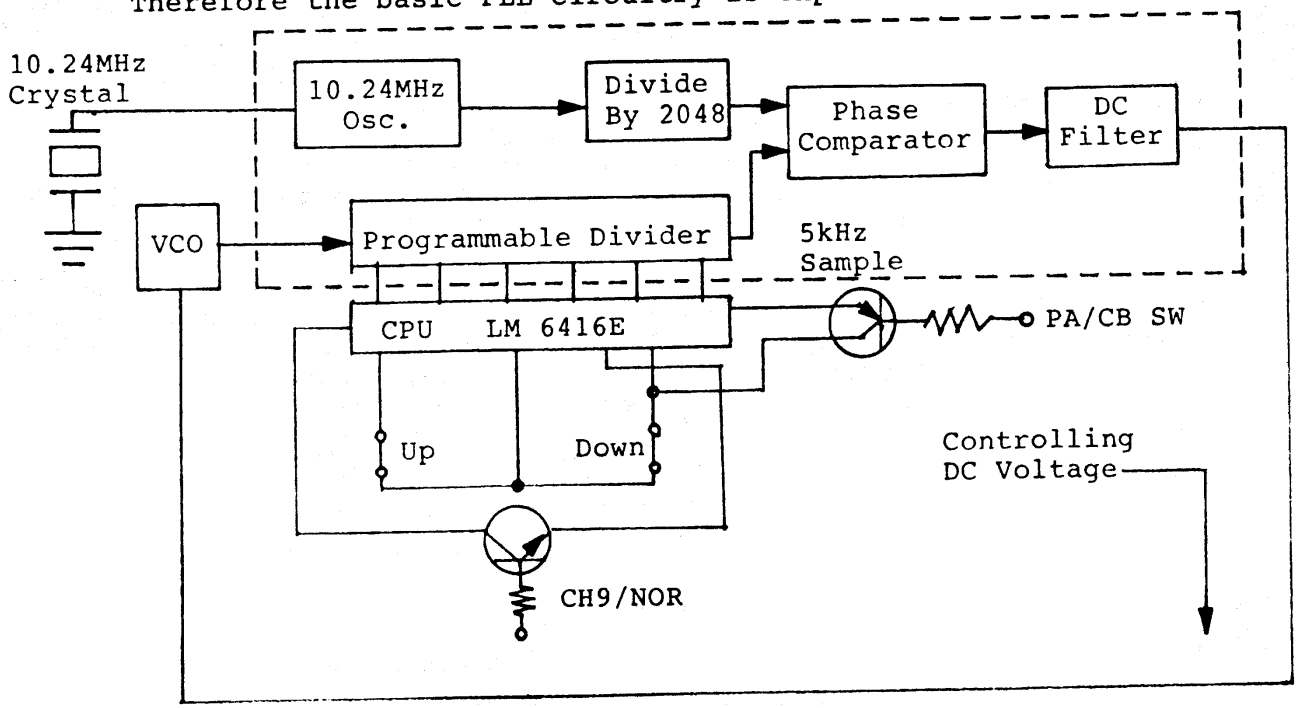
A basic PLL circuit consists of reference oscillator, VCO, phase comparator and DC filter (low pass filter).



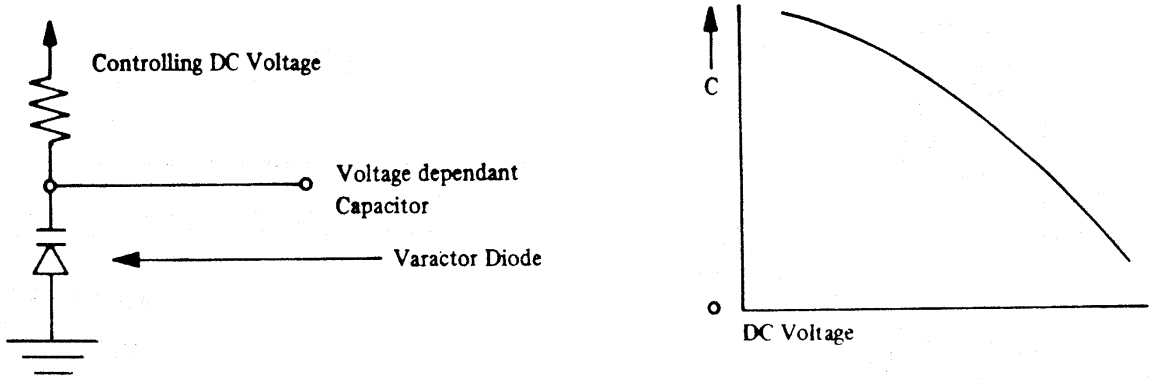
With the above circuit the VCO (Voltage Controlled Oscillator) frequency is effectively locked to the reference oscillator, and its accuracy is as good as the reference oscillator.

Since the CB radio's adjacent channel spacing is 10 kHz (or multiple of 5 kHz), our purpose should be to produce multiples of programable frequencies that are spaced apart by 10 kHz.

Therefore the basic PLL circuitry is expanded as follow:



The most important part of VCO circuitry is a voltage controlled variable capacitor called varicap or varactor diode whose capacitance depends on DC voltage applied to its cathode.



The varactor diode is responsible for setting VCO frequency, and once set it regulates the VCO frequency against the reference. The VCO frequencies are chosen in 16 to 17 MHz range as shown on table 1. To obtain transmit signal the VCO is mixed with 10.24MHz. As an example for channel 1:
10.24 + 16.725 = 26.965MHz

For receiver mode the VCO is used as a first local oscillator. Example, channel 1:
26.965 - 16.27 = 10.695MHz

The above first IF of 10.695MHz is mixed again with 10.24MHz crystal oscillator frequency which serves as the second local oscillator.
10.695 - 10.24 = 0.455MHz

As can be seen above the VCO frequency shifts from 16.725 to 16.27MHz when changed from transmit to receive for the same channel 1. The shift is accomplished by "read only memory" incorporated inside the PLL IC-202 between the selector switch and the VCO divider (programable). When transmit logic signal is applied to the IC-202 through pin 19, the programable divider will divide incoming VCO frequency by 3345 to produce 5kHz sampling signal. 16,725 ÷ 3345 = 5kHz

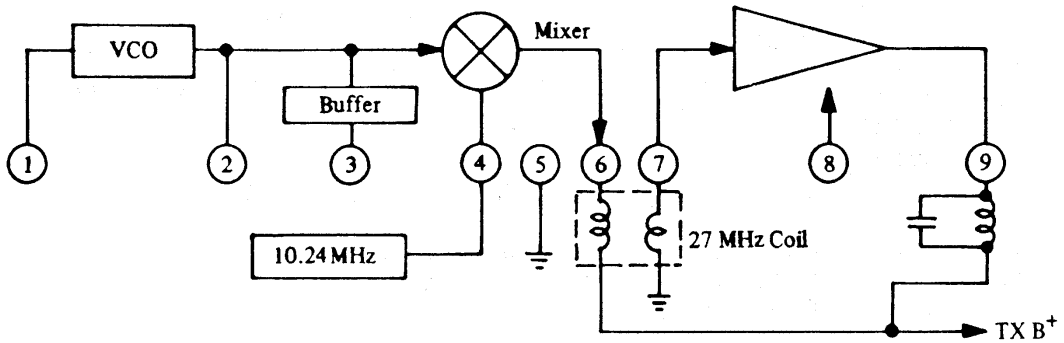
For the receiver mode the programable divider will automatically change to divide the VCO frequency by 3254.
16270 ÷ 3254 = 5kHz

Note that the reference frequency of 5kHz is obtained by dividing the 10.24MHz by 2048 times. (5kHz reference is used instead of 10kHz for division convenience). See table 1 for transmit/receive mode VCO frequencies.

2. Transmitter Circuit

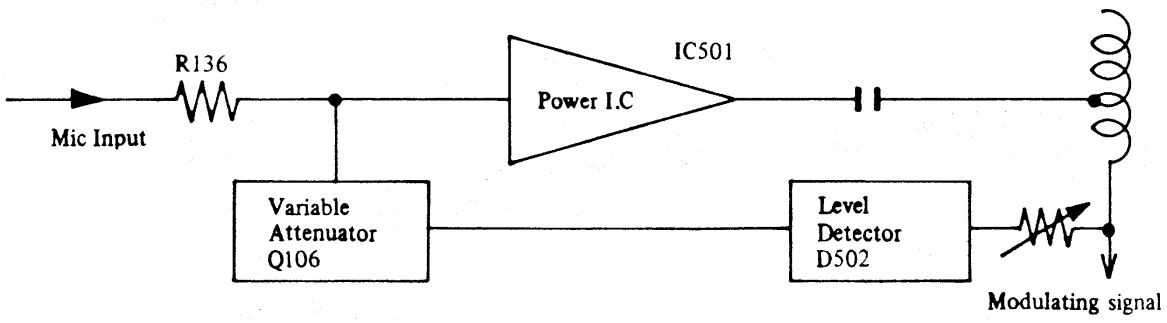
IC202 (PLL-LSI), VCO section of IC204 (pins 1,2, and 3) are operational regardless of the receive or transmit mode. When the radio is set to the transmit mode, mixer/amplifier section of IC204 (pins 4,6,7 and 9), Q203, Q301, Q302 and Q303 are activated. The VCO frequency selected by the microprocessor is mixed with 10.24MHz to generate desired transmit frequency. The mixing is done by a balanced mixer circuit located inside the IC204.

EQUIVALENT CIRCUIT OF IC204



The resulting transmit frequency from pin 9 of IC204 is filtered by L301 and L302. Q301 is an amplifier/switch circuit. When VCO frequency is out of "LOCK" condition pin 14 of IC202 pulls down bias voltage of Q301 to ground disabling Q301 from passing possible illegal frequencies. Q302 is a RF power driver circuit and Q303 is the final RF power amplifier.

A modulation audio signal is applied to the collectors of Q302 and Q303 through an audio power transformer T501. The audio signal (mic input) is amplified by a single power IC501. The modulation limiting is accomplished by an automatic level control circuit which is as follows:



L305 and C317 are series resonator, and RFC303, L307, RFC304, C321, C322, C324 and C326 make up PI-LOW pass filter. C312 is factory selected and limits the RF output level to within the FCC limit of 4 watts.

3. Receiver Circuit

In the receiver mode of operation, Q203 transistor is turned off. Also bias voltage is applied to Q103 and a proper bias and AGC voltage is established to Q101, Q102, and Q103. Q101 is a 27MHz RF input amplifier and any excessive input signal is limited by diodes D101 and D102. The amplified 27MHz is mixed with VCO frequency selected by channel switch. For channel 1 VCO is set at 16.27MHz. The resulting first IF is 26.965 - 16.27 = 10.695MHz. Q102 is the first converter, and the 10.695MHz is sharply filtered by L103 and a ceramic filter CF1. The first IF is again mixed with a second local oscillator of 10.24MHz. 10.695 - 10.24 = 0.455MHz. Q103 is the second converter. Second IF is filtered by a razor sharp ceramic filter of CF2 coupled with L104. Q104 is a first 455kHz amplifier, with Q105 being the last amplifier. D103 is a detector diode which produces audio signal as well as a negative DC voltage for AGC action. The negative voltage also provides forward biasing to the cathode of ANL clipping diode of D106. The biasing voltage has a time constant determined by R124 and C123. Therefore, any sharp negative going pulse from D103 will back bias D106 and be clipped.

4. Channel Up/Down Operation

The PLL (TX/RX) frequency, channel number display, channel 9 select, and PA/CB mode select functions are controlled by a 4 bit microprocessor. The controls for channel selection are the Up and Down push buttons located on the front panel. Depending upon which button is pressed, instructions are given to the microprocessor to change the PLL frequency to the next channel. If the button is kept in the depressed position for approximately 1.2 seconds the microprocessor will then scan through the channels at a rate of approximately 5 channels per second.

During channel selection or scan function, the microprocessor inhibits the transmitter section of the unit, to prevent undesired signals from being radiated.

FREQUENCY CHART (Table 1)

CH NO	CHANNEL FREQ(MHz)	CRYSTAL OSC	VCO TX	VCO RX
1	26.965	10.24	16.725	16.27
2	26.975	"	16.735	16.28
3	26.985	"	16.745	16.29
4	27.005	"	16.765	16.31
5	27.015	"	16.775	16.32
6	27.025	"	16.785	16.33
7	27.035	"	16.795	16.34
8	27.055	"	16.815	16.36
9	27.065	"	16.825	16.37
10	27.075	"	16.835	16.38
11	27.085	"	16.845	16.39
12	27.105	"	16.865	16.41
13	27.115	"	16.875	16.42
14	27.125	"	16.885	16.43
15	27.135	"	16.895	16.44
16	27.155	"	16.915	16.46
17	26.165	"	16.925	16.47
18	27.175	"	16.935	16.48
19	27.185	"	16.945	16.49
20	27.205	"	16.965	16.51
21	27.215	"	16.975	16.52
22	27.225	"	16.985	16.53
23	27.255	"	17.015	16.56
24	27.235	"	16.995	16.54
25	27.245	"	17.005	16.55
26	27.265	"	17.025	16.57
27	27.275	"	17.035	16.58
28	27.285	"	17.045	16.59
29	27.295	"	17.055	16.60
30	27.305	"	17.065	16.61
31	27.315	"	17.075	16.62
32	27.325	"	17.085	16.63
33	27.335	"	17.095	16.64
34	27.345	"	17.105	16.65
35	27.355	"	17.115	16.66
36	27.365	"	17.125	16.67
37	27.375	"	17.135	16.68
38	27.385	"	17.145	16.69
39	27.395	"	17.155	16.70
40	27.405	"	17.165	16.71

ALIGNMENT PROCEDURE FOR CB TRANSCEIVER
MODEL 20 PLUS

TEST EQUIPMENT REQUIRED

All Test equipment should be properly calibrated.

1. Audio Signal Generator, 10Hz - 20kHz
2. VTVM 1mV measurable.
3. DC Ammeter, 2A
4. Regulated Power Supply, dc 0-20V, 2A or higher.
5. Frequency Counter, 0-40MHz, high input impedance type.
6. RF VTVM probe type.
7. Oscilloscope, 30MHz, high input impedance.
8. RF watt meter, thermo-couple type, 50 ohm, 5W.
9. Standard Signal Generator, 100kHz-50MHz, 50 ohm unbalanced.
10. Speaker dummy resistor, 8 ohm, 5W.
11. Circuit Tester, dc, 20kV ohm/V.

TEST CONDITIONS

Test voltage = 13.8Vdc +/-5%, unless otherwise specified.

PLL CIRCUIT ALIGNMENT

a. 10.24MHz Oscillator Check

Connect a frequency counter to IC202, pin 12 and check to see 10.240000MHz +/-100Hz.

When a defective crystal is replaced and if the frequency is higher than by 100Hz, C208 should be increased. If the frequency is lower, C208 should be reduced in capacitance.

With a factory supplied crystal a C208 value of 47 pFd should be sufficient, but on some sets minor value selection may be necessary.

b. VCO Alignment

1. Set the Radio to channel 40 and into the transmit mode (make certain 50 ohm dummy load or wattmeter is connected to the antenna terminal).

2. Connect a circuit tester between TP1 and ground.

3. Adjust L201 to obtain 4.5Vdc.

4. Set the Radio to channel 1 and into the receive mode.

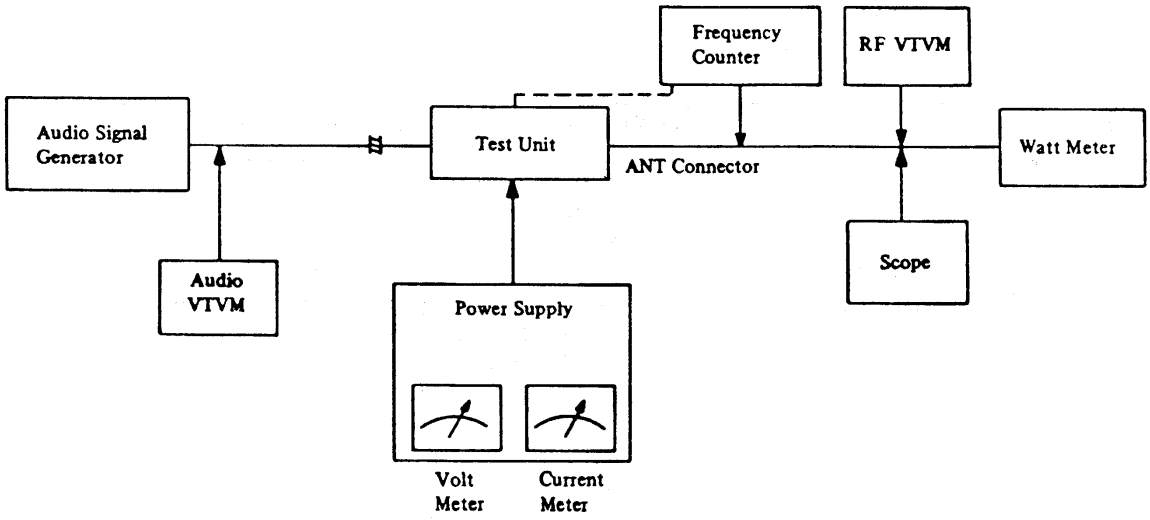
5. Check to see that the TP1 dc voltage drops to a level between 0.6 and 1.0 volts. As long as the dc level stays between 4.5Vdc for transmit on channel 40 and 0.6 to 1.0Vdc for receive on channel 1, the VCO is set properly.

   The magnitude of the TP1 voltage swing is determined by C216 at the factory. The optimum value of C216 was found to be around 82 pFd. C216 with a value larger than 82 pFd will reduce the voltage swing magnitude and vice versa for a smaller value. If the lower value drops only to 1.5Vdc, then a C216 of 82 pFd should be reduced to increase the range. This should not be necessary when factory supplied parts are used for D208 (Varactor Diode) and L201 (VCO Tuning Coil).

TRANSMITTER ALIGNMENT

a. Test Set-up

Refer to the diagram shown below:



Transmitter Alignment Set Up

Note:

1. When connecting audio cable to the microphone input circuit, always use shielded cable.

2. When making alignment for RF power output, always use the supplied dc cable.

b. RF Amplifier Stage Alignment

1. Reduce power supply voltage to 9.0V.

2. Set channel selector to 19 and connect the oscilloscope to the antenna connector through a suitable connection pad.

3. Adjust L301, L302, L303 and L304 for maximum amplitude of the scope display.

4. Increase the power supply voltage to 13.8V, and then adjust L305 and L307 until the watt meter indicates 3.8W.

5. Measure the transmit power output at all channels, and make sure that the power output difference between any channels is less than 0.3W.

6. Measure the transmit frequency at all channels, and make sure that the frequency is within +/-800Hz from the assigned channel center frequencies.

c. Transmit Frequency Check

1. Set the radio into transmit mode with no modulation.

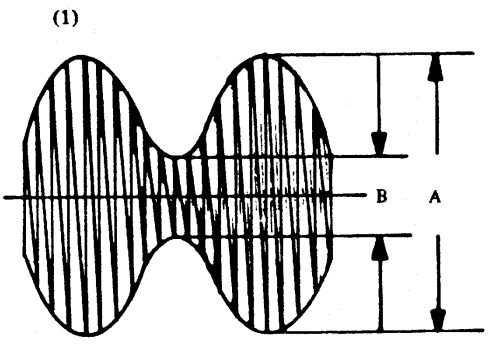
2. Connect the frequency counter to the antenna load or to the tab provided at the watt meter.

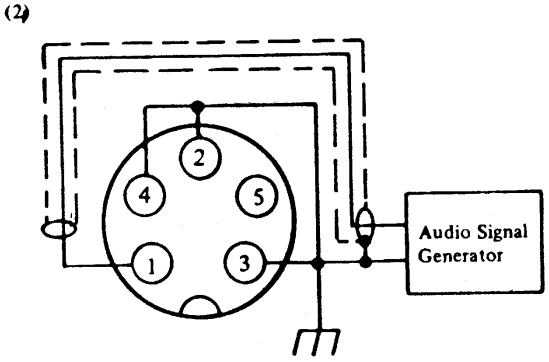
   The frequency should be within +/-800Hz from each channel center frequency as tabulated in Table 1.

d. Modulation Sensitivity Alignment

1. Set the unit to transmit mode of operation. Feed 1kHz, 30mV signal to the microphone input circuit, and adjust RV501 so that 100% modulation is obtained.

2. To set the transceiver into transmit mode without a microphone, insert the plug, wired as shown below, into the MIC jack on the transceiver. When applying the audio modulation signal to the microphone input circuit, use the same plug.





Modulation ratio = $\frac{A-B}{A+B}$ x 100 (%)

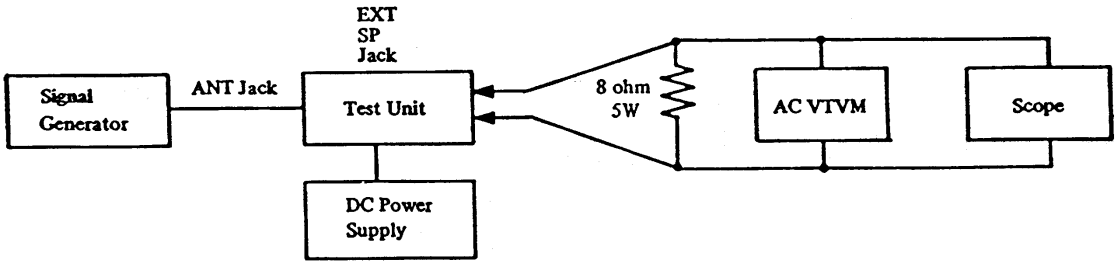
Mic Plug wiring for modulation

3. Next, reduce the signal input level to 3 mV, and make sure that the modulation is higher than 60%.

RECEIVER CIRCUIT ALIGNMENT

a. Test Set-up

Refer to the diagram shown below:



RECEIVER ALIGNMENT SETUP

b. Sensitivity Alignment

1. Set the signal generator to provide 27.185MHz, 1kHz, 30% modulation. Set the channel selector to 19.

2. Adjust L101, L102, L103, L104 and L105 for maximum audio output across the 8 ohm dummy load resistor. This alignment should be performed by gradually decreasing the generator output signal to the minimum level required for tuning to avoid inaccurate alignment due to AGC action.

c. Squelch Circuit Alignment

1. Set a 50 ohm signal generator to generate a signal on channel 19 with an output level of 1000 microvolts, modulated 30% with a 1kHz tone.

2. Rotate the squelch control in full clockwise direction.

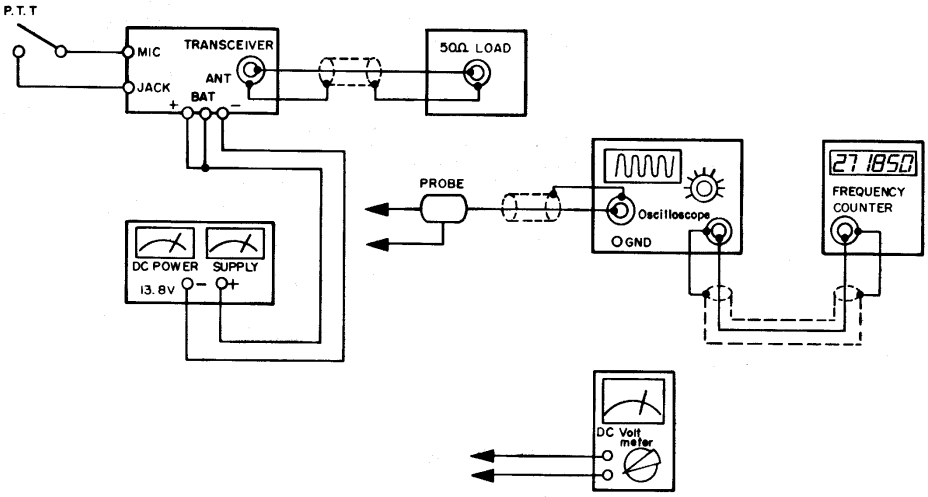
3. Temporarily adjust RV101 for maximum audio output, and note the audio output level. Then adjust RV101 so that the audio output level decreases by 6db.

4. Next, reduce the antenna input signal level to between 794 and 447 microvolts. The receiver should squelch. (The audio output level should drop to zero.)

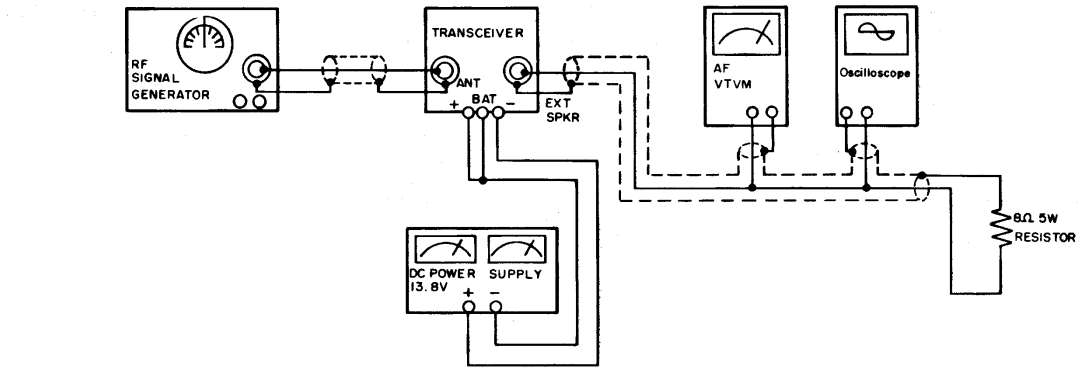
5. Reduce the antenna signal input level to zero, and adjust the SQ control until the noise output just disappears.

Test Equipments Setup

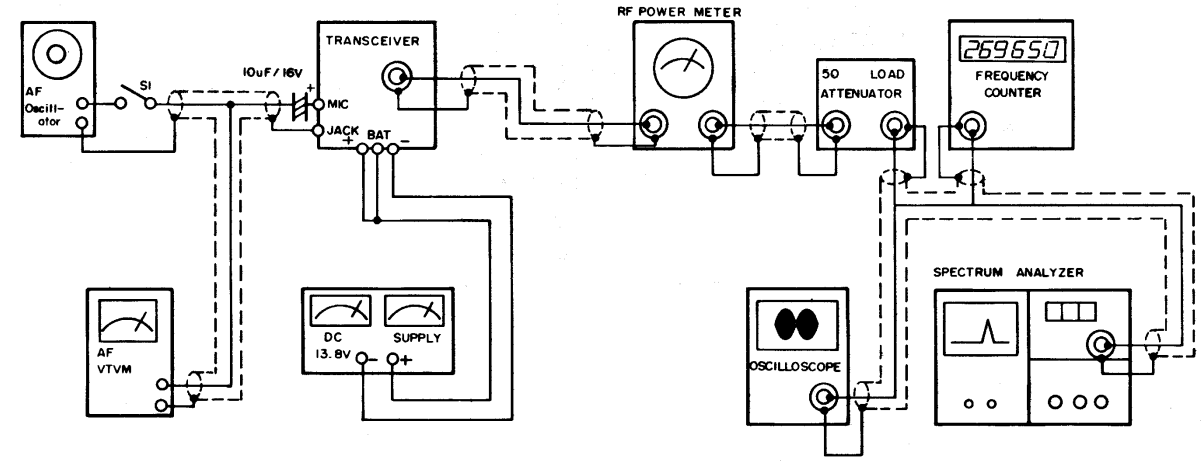
PLL AND CARRIER SECTION



RECEIVER SECTION



TRANSMITTER SECTION



Voltage Chart

CONDITIONS MEASURED ON CH19
NO SIGNAL
NO MODULATION

1) TRANSISTORS

TR NO		B	E	C
Q101	RX	1.65	0.96	12.80
	TX	0.34	3.94	12.72
Q102	RX	1.63	0.90	11.85
	TX	0.24	0	12.70
Q103	RX	1.60	1.01	11.0
	TX	0.34	0.01	12.67
Q104	RX	1.07	0.38	3.29
	TX	0.09	0	0.81
Q105	RX	3.29	2.59	12.90
	TX	0.81	0.17	12.67
Q106	SQH	0.7	0	0
	SQL	0		
	TX	0	0	0.06
Q107	RX	0.62	0	0.71
	TX	0.62	0	0.71

TR NO		B	E	C
Q201	RX	7.82	8.05	2.51
	TX	7.81	8.20	2.48
Q202	RX	7.78	8.05	2.53
	TX	7.84	8.10	2.56
Q203	RX	7.95	7.95	0.91
	TX	7.16	7.94	7.81
Q204	RX	6.43	3.07	0
	PA	4.81	5.46	5.45
	TX	6.46	3.08	0.04
Q205	RX	0	0	3.08
	TX	0	0	3.11
Q301	RX	0.33	0	13.18
	TX	1.39	0.81	12.87
Q302	RX	0	0	13.5
	TX	0	0	10.61

TR NO		B	E	C
Q303	RX	0	0	13.10
	TX	0	0	11.74
Q401	RX	5.78	5.16	13.18
	TX	5.78	5.14	13.03
Q402	RX	7.94	7.95	0
	TX	7.93	7.94	0
Q403	RX	0	0	0
	TX	0	0	0
Q404	RX	0.42	0	7.80
	TX	0.40	0	7.79
Q501	SQH	0.37	0	2.51
	SQL	0.68	0	0.05
	TX	0.68	0	0.05
Q502	SQH	0.65	0	0
	SQL	0.19	0	0.68
	TX	0.1	0	0.68

2) IC

IC NO	IC 201													
PIN	1	2	3	4	5	6	7	8	9	10	11	12	13	14
RX	0.21	0.21	2.38	6.0	2.0	2.0	NC	5.13	6.44	0.07	0.07	6.46	0	0
TX	0.21	0.22	0.41	5.93	2.05	2.0	NC	5.15	6.49	0.07	0.07	6.50	0	0
PIN	15	16	17	18	19	20	21	22	23	24	25	26	27	28
RX	6.45	0.07	8.11	0.03	5.92	5.14	0	0	0	0.67	3.08	3.08	5.23	3.08
TX	6.49	0.07	8.1	0.03	5.88	5.16	0	0	0	7.81	3.11	3.10	5.28	3.08

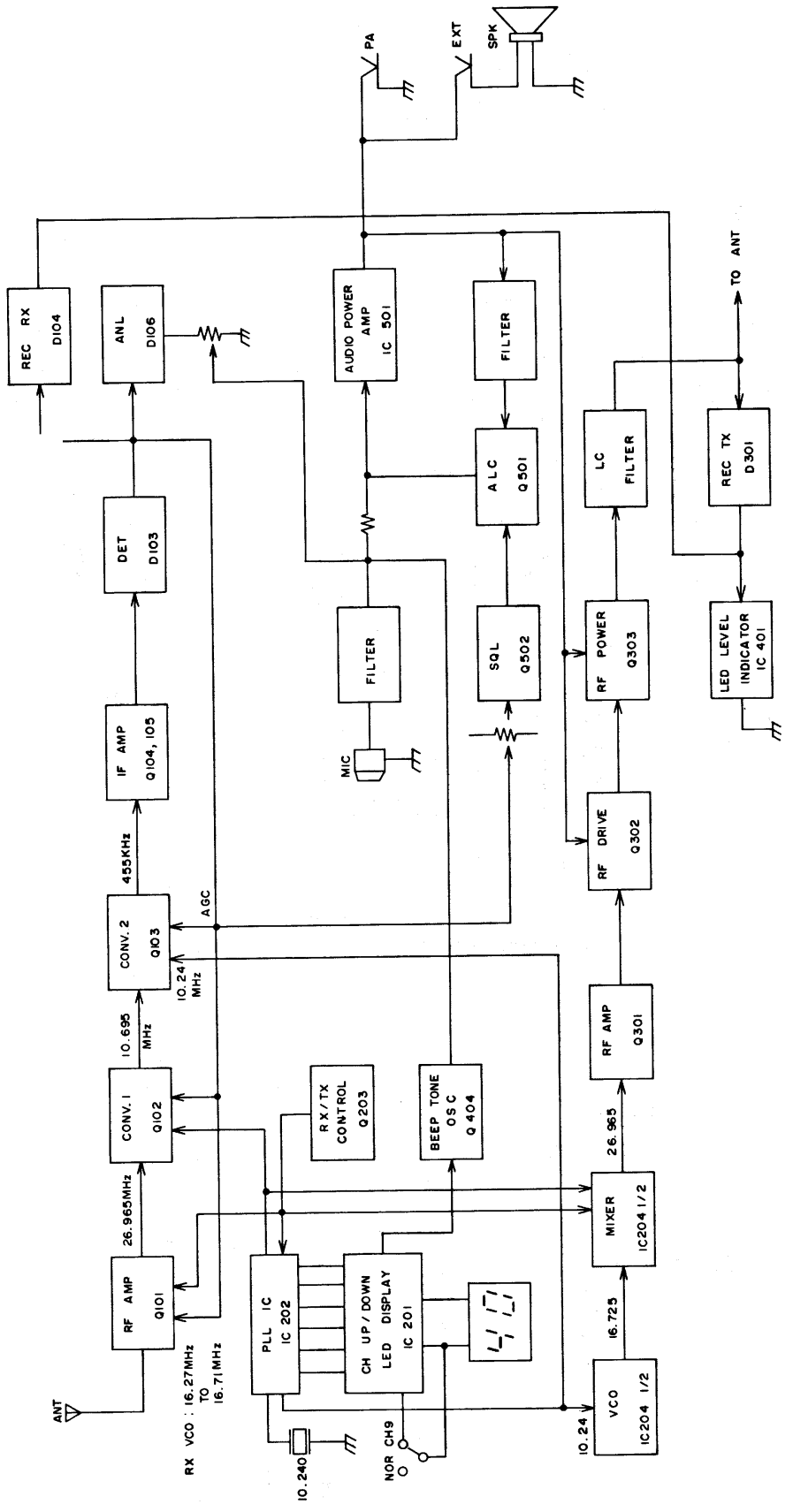
IC NO	IC 202										IC401			
PIN	1	2	3	4	5	6	7	8	9	10	1	2	3	4
RX	6.44	0.07	0.07	6.46	6.45	0.07	NC	NC	NC	1.45	0	10.81	11.45	10.75
TX	6.48	0.07	0.07	6.50	6.49	0.07	NC	NC	NC	4.10	0	0.06	0.06	0.07
PIN	11	12	13	14	15	16	17	18	19	20	5	6	7	8
RX	2.83	3.83	0	1.45	1.74	1.74	1.37	7.57	3.85	7.19	10.88	11.15	12.80	0
TX	3.23	3.83	0	4.10	1.60	1.61	3.06	7.59	3.31	0.81	0.08	0.08	11.55	1.31

IC NO	IC203			IC501									
PIN	1	2	3	1	2	3	4	5	6	7	8	9	10
RX	2	0	0	13.80	12.60	3.90	8.15	1.51	3.38	3.40	1.28	0	6.86
TX	3	7.95	7.94	13.50	12.28	3.90	8.02	1.51	3.30	3.33	1.27	0	6.72

IC NO	IC 205													
PIN	1	2	3	4	5	6	7	8	9	10	11	12	13	14
RX	0	4.8	5	0	4.8	0	0	NC	NC	NC	NC	NC	NC	5
TX	0	4.8	5	0	4.8	0	0	NC	NC	NC	NC	NC	NC	5

IC NO	IC 204								
PIN	1	2	3	4	5	6	7	8	9
RX	2.64	1.96	1.37	1.78	0	1.27	2.12	5.10	1.27
TX	2.56	1.90	1.37	2.56	0	7.08	2.02	5.50	7.08

Block Diagram



PLL Circuit Block Diagram