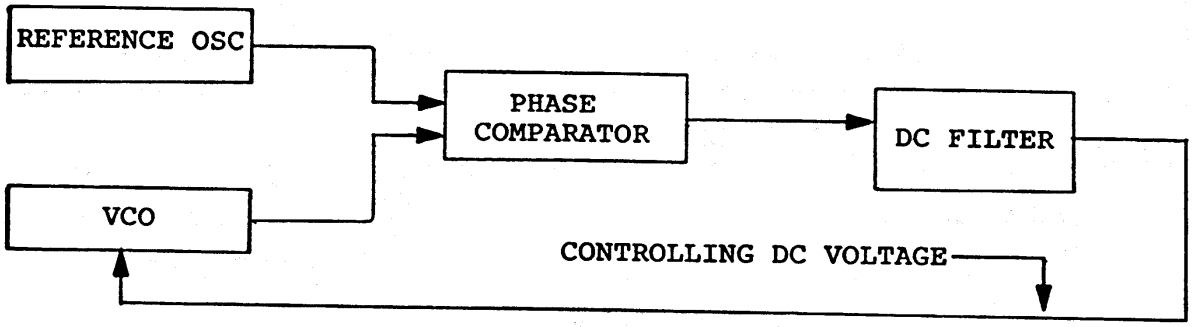
TABLE OF CONTENTS
Model 40 Plus

OPERATING THEORY OF PLL FREQUENCY SYNTHESIZER
FOR MODEL 40 PLUS

1. Fundamental Theory Of PLL Circuitry

The purpose of PLL (Phase Locked Loop) circuit is to generate multiple number programable frequencies from a signal reference frequency with quartz crystal accuracy.

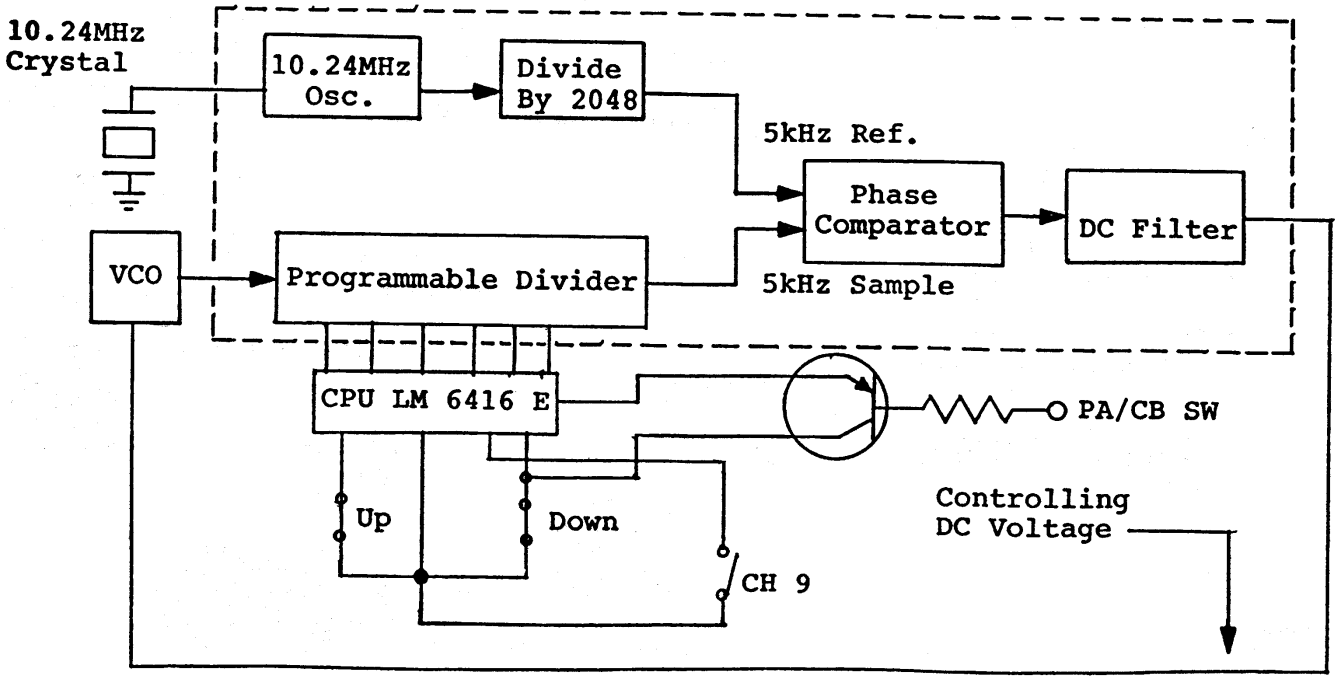
A basic PLL circuit consists of reference oscillator, VCO, phase comparator and DC filter (low pass filter).



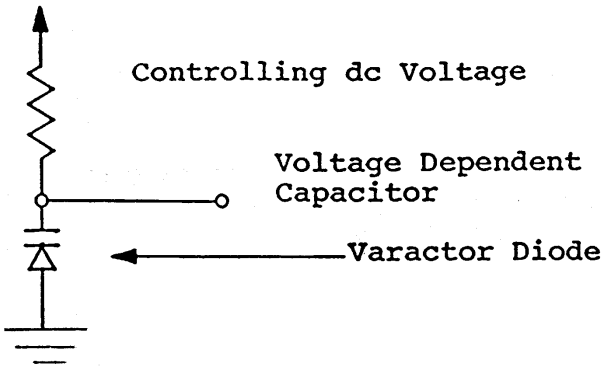
With the above circuit the VCO (Voltage Controlled Oscillator) frequency is effectively locked to the reference oscillator, and its accuracy is as good as the reference oscillator.

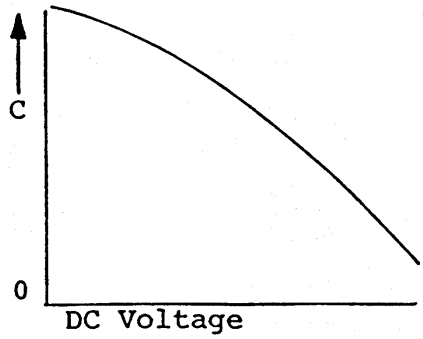
Since the CB radio's adjacent channel spacing is 10 kHz (or multiple of 5 kHz), our purpose should be to produce multiples of programable frequencies that are spaced apart by 10 kHz.

Therefore the basic PLL circuitry is expanded as follow:



The most important part of VCO circuitry is a voltage controlled variable capacitor called varicap or varactor diode whose capacitance depends on DC voltage applied to its cathode.





The varactor diode is responsible for setting VCO frequency, and once set it regulates the VCO frequency against the reference. The VCO frequencies are chosen in 16 to 17 MHz range as shown on table 1. To obtain transmit signal the VCO is mixed with 10.24MHz. As an example for channel 1:
10.24 + 16.725 = 26.965MHz

For receiver mode the VCO is used as a first local oscillator. Example, channel 1:
26.965 - 16.27 = 10.695MHz

The above first IF of 10.695MHz is mixed again with 10.24MHz crystal oscillator frequency which serves as the second local oscillator.
10.695 - 10.24 = 0.455MHz

As can be seen above the VCO frequency shifts from 16.725 to 16.27MHz when changed from transmit to receive for the same channel 1. The shift is accomplished by "read only memory" incorporated inside the PLL IC-202 between the selector switch and the VCO divider (programable). When transmit logic signal is applied to the IC-202 through pin 19, the programable divider will divide incoming VCO frequency by 3345 to produce 5kHz sampling signal. 16,725 ÷ 3345 = 5kHz

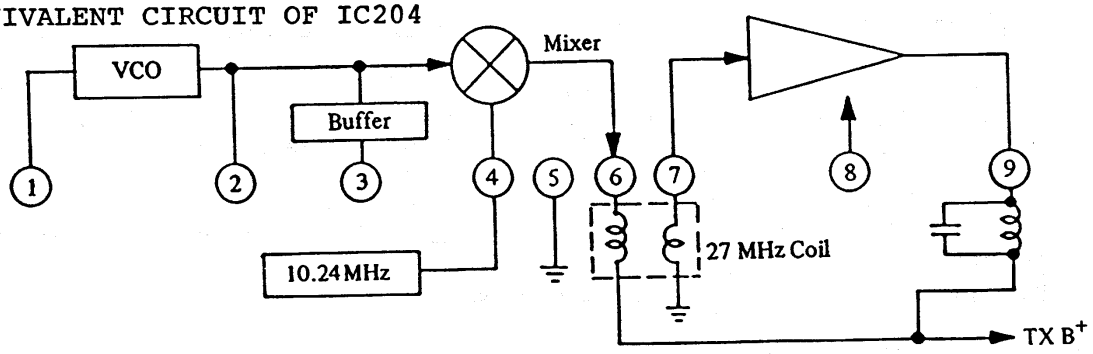
For the receiver mode the programable divider will automatically change to divide the VCO frequency by 3254.
16270 ÷ 3254 = 5kHz

Note that the reference frequency of 5kHz is obtained by dividing the 10.24MHz by 2048 times. (5kHz reference is used instead of 10kHz for division convenience). See table 1 for transmit/receive mode VCO frequencies.

2. Transmitter Circuit

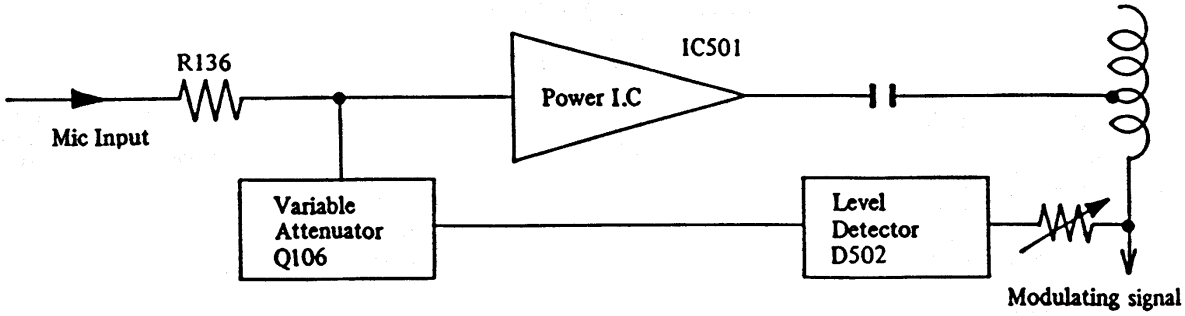
IC203 (PLL-LSI), VCO section of IC203 (pins 1,2, and 3) are operational regardless of the receive or transmit mode. When the radio is set to the transmit mode, mixer/amplifier section of IC204 (pins 4,6,7 and 9), Q203, Q301, Q302 and Q303 are activated. The VCO frequency selected by the microprocessor is mixed with 10.24MHz to generate desired transmit frequency. The mixing is done by a balanced mixer circuit located inside the IC203.

EQUIVALENT CIRCUIT OF IC204



The resulting transmit frequency from pin 9 of IC204 is filtered by L301 and L302. Q301 is an amplifier/switch circuit. When VCO frequency is out of "LOCK" condition pin 14 of IC202 pulls down bias voltage of Q301 to ground disabling Q301 from passing possible illegal frequencies. Q302 is a RF power driver circuit and Q303 is the final RF power amplifier.

A modulation audio signal is applied to the collectors of Q302 and Q303 through an audio power transformer T201. The audio signal (mic input) is amplified by a single power IC206. The modulation limiting is accomplished by an automatic level control circuit which is as follows:



L305 and C339 are series resonator, and L306, L307, C361, and C342 make up PI-LOW pass filter. C335 is factory selected and limits the RF output level to within the FCC limit of 4 watts.

3. Receiver Circuit

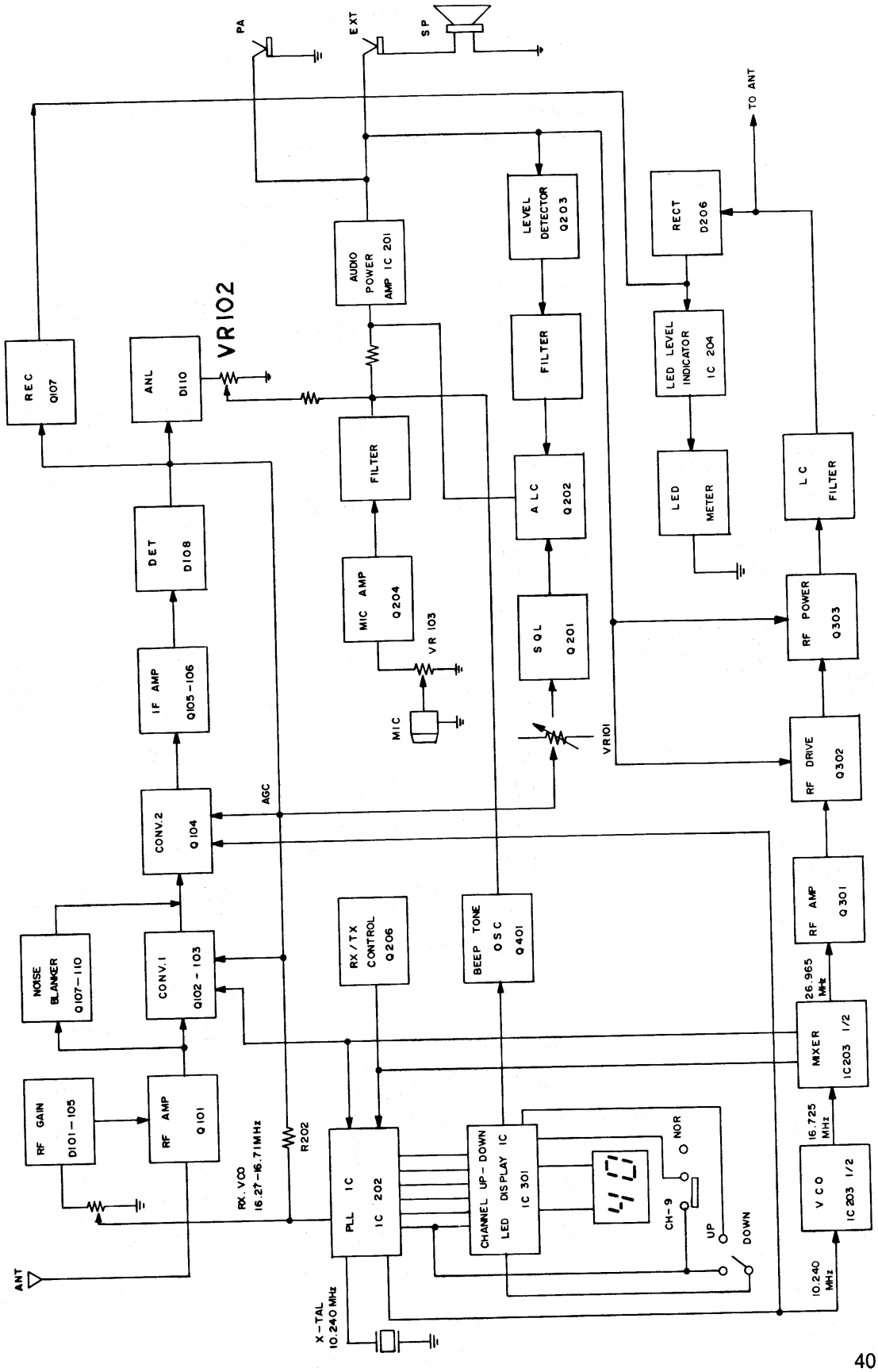
In the receiver mode of operation, Q206 transistor is turned off. Also bias voltage is applied to Q105 and a proper bias and AGC voltage is established to Q101, Q102, Q103 and Q105. Q101 is a 27MHz RF input amplifier and any excessive input signal is limited by diodes D101 and D105. The amplified 27MHz is mixed with VCO frequency selected by channel switch. For channel 1 VCO is set at 16.27MHz. The resulting first IF is 26.965 - 16.27 = 10.695MHz. Q102 and Q103 is the first converter, and the 10.695MHz is sharply filtered by L103 and a ceramic filter CF1. The first IF is again mixed with a second local oscillator of 10.24MHz. 10.695 - 10.24 = 0.455MHz. Q104 is the second converter and the 455kHz. Second IF is filtered by a razor sharp ceramic filter of CF2 coupled with L105. Q105 is a first 455kHz amplifier, with Q106 being the last amplifier. D108 is a detector diode which produces audio signal as well as a negative DC voltage for AGC action. The negative voltage also provides forward biasing to the cathode of ANL clipping diode of D110. The biasing voltage has a time constant determined by R126 and C121. Therefore, any sharp negative going pulse from D108 will back bias D110 and be clipped.

4. Channel Up/Down Operation

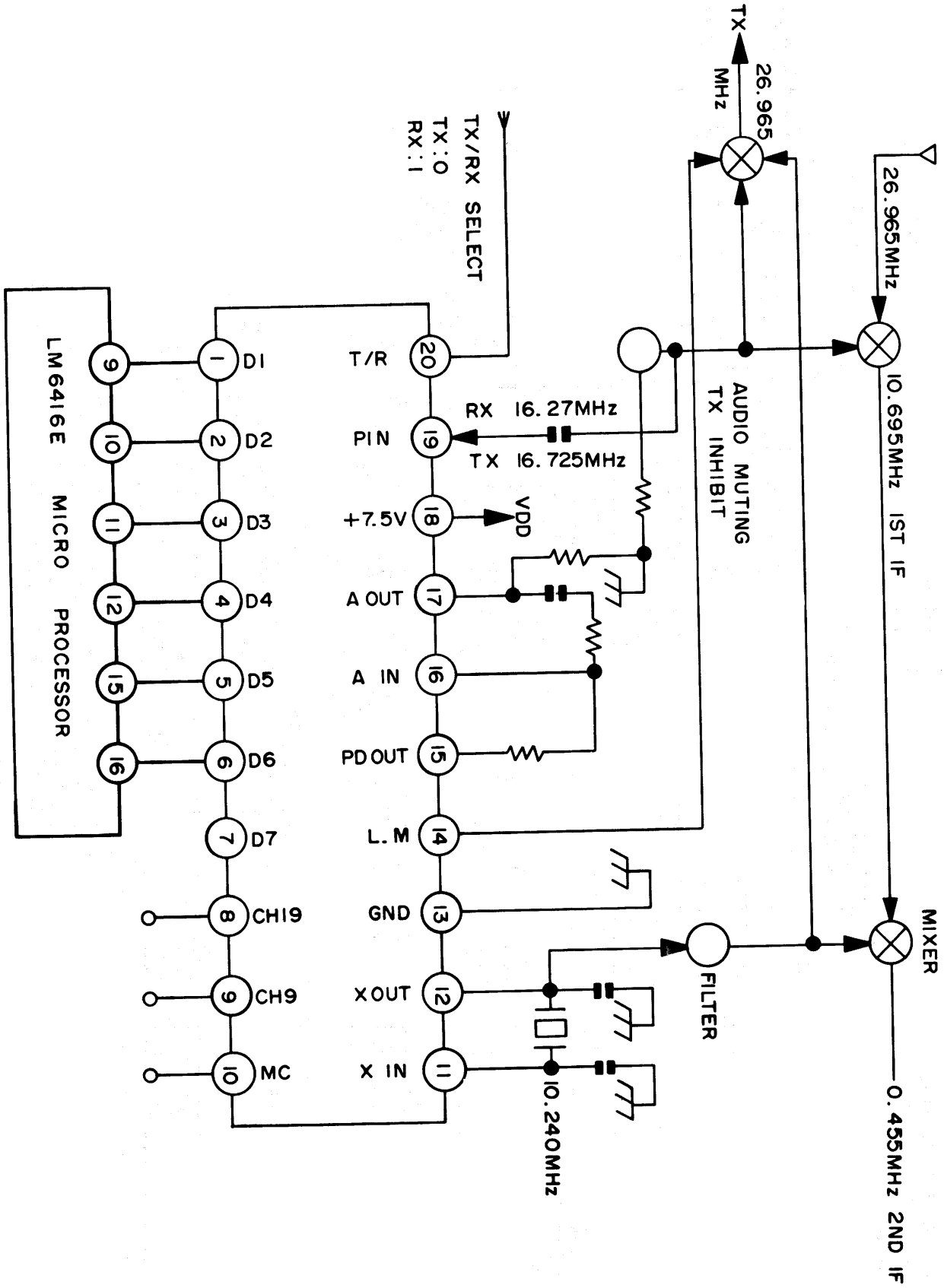
The PLL (TX/RX) frequency, channel number display, channel 9 select, and PA/CB mode select functions are controlled by a 4 bit microprocessor. The controls for channel selection are the Up and Down push buttons located on the front panel. Depending upon which button is pressed, instructions are given to the microprocessor to change the PLL frequency to the next channel. If the button is kept in the depressed position for approximately 1.2 seconds the microprocessor will then scan through the channels at a rate of approximately 5 channels per second.

During channel selection or scan function, the microprocessor inhibits the transmitter section of the unit, to prevent undesired signals from being radiated.

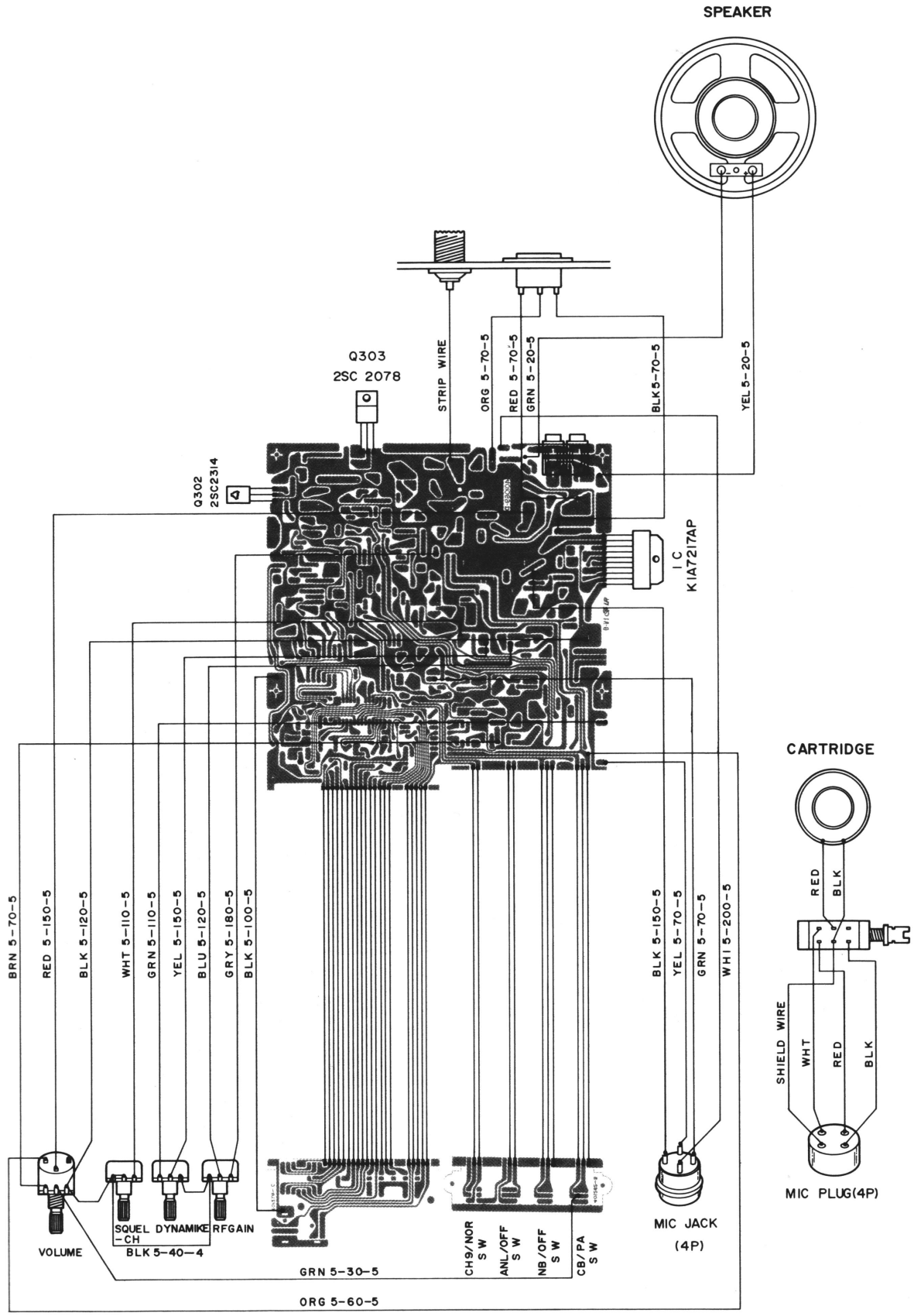
Block Diagram



PLL Circuit Block Diagram



Wiring Diagram



P.C.B Wiring Diagram